SIMULATION OF NONLINEAR CIRCUITS WITH GENERAL CIRCUIT TOPOLOGY

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Abstract This report describes a milestone in the development of the McCAE system, namely the generalization of circuit topology for the simulation and optimization of nonlinear microwave circuits. The program now accommodates circuits with multiple nonlinear devices and different device topologies such as diodes and FETs. This capability facilitates the evolution of McCAE from a device simulator into a circuit simulator. The McCAE formulation of a general circuit topology is described. The key data structures for device and circuit simulation and the corresponding numerical procedures are discussed. Examples of diode circuits, quadratically nonlinear circuits and distributed amplifiers are provided.

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I. INTRODUCTION

It is our goal to establish a next-generation CAD engine for simulation and optimization of general linear and nonlinear circuits. Through rigorous research in this area we have derived a unified theory for frequency domain linear/nonlinear simulation and sensitivity analysis [1], and presented state-of-the-art results in simultaneous DC/small-signal based nonlinear parameter extraction [2] and harmonic balance (HB) based large-signal parameter extraction [3]. These significant results form the foundation of our next-generation CAD system.

Combining various highly efficient techniques in a coherent CAD system is essential. In the first step, we established the research software system McCAE, which simulates and optimizes nonlinear circuits with one nonlinear FET device and an arbitrary topology of the linear subcircuit.

The capability of accommodating multiple nonlinear devices and arbitrary device topology, such as diodes and dual-gate FETs, is a crucial step towards our goal of establishing a general purpose CAD tool. Such upgrades to the program requires restructuring of several key data structures related to circuit simulation and modifications of many routines related to HB simulation, DC/small-signal simulation, device library, etc. The work has been successfully carried out and verified. This report examines the major steps in the work, describes several key data structures and overviews the circuit simulation and optimization process. Small- and large-signal simulation and optimization are applied to diode, distributed amplifier and quadratically nonlinear circuits. Circuit input files and response plots for the examples are also provided.

In this report, the phrase "circuit simulation" (or "circuit optimization") refers to the simulation (or optimization) of either a DC/small-signal circuit or a large-signal circuit or a combination of both. Small-signal simulation is done by first linearizing the nonlinear devices at a bias point and then performing a linear circuit simulation.

II. DESCRIPTION OF A GENERAL McCAE CIRCUIT

Consider a general nonlinear circuit shown in Fig. 1. The circuit consists of a linear part and several nonlinear devices. A generic representation of a nonlinear device is shown in Fig. 2. The linear part of the circuit can include, e.g., matching circuits and bias circuits. The topology in the linear part is arbitrary. In a circuit simulation, the nodes in the linear part are classified as input/output nodes, bias nodes, nonlinear nodes and internal nodes. The bias nodes refer to the connection nodes between bias sources and the circuit. The nonlinear nodes refer to the connection nodes between the linear part and nonlinear devices. Any node which does not belong to input/output nodes, bias nodes and nonlinear nodes is considered an internal node.

In circuit simulation, McCAE performs a reduction of the linear part of the circuit by suppressing the internal nodes and at the same time converting the circuit matrix from a nodal formulation into a port formulation. We define the following variables which are used in the source code of the program:

NPOR2: total number of nonlinear ports

NPOR3: total number of nonlinear ports, bias ports and input/output ports

NPOR5: total number of bias ports

The input/output and the bias ports are formulated according to user-specified information in the circuit file. The nonlinear ports are formulated by referring each device node (except a designated reference node) w.r.t. a designated reference node in the device (see Fig. 2). In a multi-device circuit, each device has its own reference node.

The size of the reduced circuit matrix (reduced Y matrix) is NPOR3 by NPOR3. The sequence of the corresponding ports (NPOR3 corresponding ports in total) are: nonlinear ports first (NPOR2 nonlinear ports), bias ports second (NPOR5 bias ports) and input/output ports last. Therefore, rows (or columns) 1, 2, ..., NPOR2 in the reduced Y matrix correspond to nonlinear ports. Rows (or columns) NPOR2 + 1, NPOR2 + 2, ..., NPOR2 + NPOR5 in the reduced Y matrix correspond to bias ports. Rows (or columns) NPOR2 + NPOR5 + 1, NPOR2 + NPOR5 + 2, ..., NPOR3 in the reduced Y matrix correspond to input/output ports.

Each bias source must be a DC source while input sources can be at any frequency other than DC. Linearization of a nonlinear device is done at the operating bias conditions while all input excitations are held at zero value.

III. KEY DATA STRUCTURE AND VARIABLES FOR CIRCUIT SIMULATION

Of primary importance in developing a circuit simulator is the data structure for variables, parameters, device node numbers, etc. Such information is stored in an array named IFLAGS() and is defined in the include file "flag.inc". This array is described as follows.

Let NDEV be the total number of nonlinear devices in the circuit. The integer quantity IFLAGS(*, i) contains necessary information related to the ith device, i = 1, 2, ..., NDEV.

IFLAGS(1, i) : Element number (presently not used but reserved for future use).

IFLAGS(2, i) : Model code for the ith device. Each device model has a code, e.g, 1001 for the Curtice FET model, 1010 for a user-defined one-port model.

IFLAGS(3, i) : Number of nonlinear ports of the ith device. This is equal to the number of intrinsic nodes excluding the reference node in the device.

IFLAGS(4, i) : Offset of nonlinear port indices of the ith device as seen from the overall circuit. For the overall circuit, the total number of nonlinear ports is NPOR2. The jth port of the ith device is the (IFLAGS(4, i) + j)th nonlinear port in the overall circuit.

IFLAGS(5, i) : Number of branches in the ith device. All branches in a device are considered nonlinear branches in the overall circuit.

IFLAGS(6, i) : Offset of branch indices of the ith device as seen from the overall circuit. For the overall circuit, the total number of nonlinear branches is NELE. The jth branch of the ith device is the (IFLAGS(6, i) + j)th nonlinear branch in the overall circuit.

IFLAGS(7, i) : Number of linearized elements of the ith device. When a nonlinear device is used for small-signal analysis, all branches in the device are linearized. The number of linearized elements is usually larger than the number of branches in a device. This is further discussed towards the end of this section.

IFLAGS(8, i) : Offset of linearized element indices of the ith device as seen from the overall circuit. For the overall circuit, the total number of linearized elements is NELEJ. The jth linearized element of the ith device is the (IFLAGS(8, i) + j)th linearized element in the overall circuit.

IFLAGS(9, i) : Number of model parameters in the ith device.

IFLAGS(10, i) : Offset of model parameter indices of the ith device as seen from the overall circuit. The jth model parameter of the ith device is the (IFLAGS(10, i) + j)th model parameter in the overall circuit.

IFLAGS(11, i) : Number of time delay parameters in the ith device.

IFLAGS(12, i) : Offset of time delay indices of the ith device as seen from the overall circuit. For the overall circuit, the total number of time delay parameters is NTAU. The jth time delay parameter of the ith device is the (IFLAGS(12, i) + j)th time delay parameter in the overall circuit.

IFLAGS(13, i) : Index of the first time delay parameter in the ith device as seen from all the model parameters of this device. For example, if the ith device has 20 model parameters in which the 16th and the 17th are time delay parameters, then IFLAGS(13, i) = 16.

For the overall circuit, the array containing all model parameters of all nonlinear devices is PA(*), also defined in the include file "flag.inc". PA(i) contains the ith model parameter as seen from the entire circuit. Using information in IFLAGS(9, *) and IFLAGS(10, *), one can find which parameter of which device PA(i) belongs to.

The array storing nonlinear branch information is INDD(*, *), defined in the include file "flag.inc". The total number of nonlinear branches in the overall circuit is NELE. The ith nonlinear branch is connected to nodes INDD(1, i) and INDD(2, i). The nonlinear function for the ith branch is a current function (e.g., representing a nonlinear resistor or nonlinearly controlled current source) if INDD(3, i) = 1 or a charge function (representing a nonlinear capacitor) if INDD(3, i) = -1.

For the overall circuit, the array storing linearized elements is ELEJAC(*, *). The array storing the topological information of linearized elements is NODJAC(*, *). Both arrays are defined in the include file "flag.inc". The total number of linearized elements in the circuit is NELEJ. For the ith linearized element in the circuit, ELEJAC(k, i) contains the value (e.g., transconductance, conductance, capacitance) of this linearized element at either the kth time sample point (if used before the Fourier transform on ELEJAC) or the kth harmonic (if used after the Fourier transform). NODJAC(1, i) to NODJAC(4, i) contain the node indices to which the linearized element is connected. Generally, the linearization of a nonlinear branch is done by differentiating the branch current (or branch charge if the branch is capacitive) w.r.t. a controlling voltage. The branch current (or charge) flows from nodes NODJAC(1, i) to NODJAC(2, i). The controlling voltage is between nodes NODJAC(3, i) and NODJAC(4, i). If a nonlinear branch is controlled by more than one voltage variables, the branch has to be differentiated w.r.t. each and every one of the controlling voltages. Therefore, there may be more linearized elements than nonlinear branches.

IV. OVERVIEW OF THE McCAE APPROACH TO CIRCUIT SIMULATION WITH GENERAL LINEAR AND NONLINEAR TOPOLOGY

Our work on HB simulation and sensitivity analysis [1, 3] and on integrated nonlinear based DC/small-signal modeling [2] have established the foundation for an integrated and nonlinearly based DC/small-signal/large-signal simulator. This section reviews the subject from an implementation point of view. We summarize important steps of circuit simulation and optimization with emphasis on the application to multi-device circuits with generalized topology.

The Starting Point for HB Simulation

HB is an iterative procedure to find the voltage (or current) spectrum at all the nonlinear ports. A good starting point for these voltage variables will speed up HB simulation. In a single FET circuit, the unknown voltage variables are intrinsic gate and drain voltages. It is relatively easy to relate the starting values for these variables to the given bias conditions and the given input power levels. For example, we can assume 90% of the drain bias voltage as the starting value for the unknown intrinsic drain voltage at DC. For circuits with multiple devices and arbitrary devices, e.g., diodes, dual-gate FETs, etc., the relation between bias conditions and the starting point of unknown voltage variables becomes complicated. In this case we initialize the unknowns for the first device the same way as in a single device circuit. For other devices in the circuit we assign a small value for all the unknowns.

Initialization of Fourier Transform Coefficients

For a general nonlinear device model or a multi-device circuit, there may be multiple time delay parameters. For example, a dual-gate FET may have two different time delay parameters. In the Fourier transform a delayed waveform is computed with a predetermined set of coefficients. A 2-dimensional array WTAU(*, *) is created to store such coefficients. WTAU(*, *) is defined in the include file "dft.inc". WTAU(k, i) is the coefficient computed from the ith time delay parameter for the kth harmonic component. Such coefficients are used in each iteration of the HB procedure.

Computation of Nonlinear Currents and Charges

The Fourier transform is applied to the starting values of the nonlinear port voltage spectrum, resulting in time domain waveforms including delayed waveforms. While in the time domain, all branches of each nonlinear device are processed. Each branch can be represented by a current function or a charge function. Then the results are transformed into the frequency domain. The branch current spectrum or charge spectrum are assembled into the HB equations using the topological information in array INDD(*, *). The driving subroutine for this purpose is *MODEL*.

Computation of Jacobian Matrix for HB Equations

We differentiate the current or charge of each and every branch of each and every nonlinear device w.r.t. their controlling voltages. Such derivative information is then stored into array ELEJAC(*, *). Using the topological information in NODJAC(*, *), the values in ELEJAC(*, *) are assembled into a Jacobian matrix for the HB equation. The branches affected by time delay parameters are assembled into the Jacobian matrix with additional computations involving WTAU(*, *) and operations with split real/imaginary variables. Such numerical procedure is organized in subroutines *JAC_HB*, *JACOB0* and *JACQ*.

Small-Signal Simulation and Sensitivity Analysis

For small-signal simulation, McCAE first solves the circuit at its DC bias conditions. Then all the nonlinear devices are linearized at the bias point. The derivative information stored in array ELEJAC(*, *) represents conductances, transconductances and capacitances which are linearized from the nonlinear device characteristics. They are assembled into the reduced circuit matrix (reduced Y matrix) according to the topological information stored in NODJAC(*, *). The resulting admittance matrix then becomes the overall circuit matrix including both the linear and the nonlinear parts. The S-parameters are calculated from this matrix.

The derivatives of S-parameters w.r.t. circuit variables are computed according to the chain rule. Several intermediate derivatives are involved including derivatives of S-parameters w.r.t. the Z matrix of the circuit, the Z matrix w.r.t. the Y matrix, the Y matrix w.r.t. solutions of the DC circuit, the Y matrix w.r.t. to optimization variables, and adjoint sensitivity of the DC solution w.r.t. optimization variables.

Circuit Simulation and Optimization

There are two types of nonlinear circuit equations handled by McCAE, namely the HB equations for large-signal analysis and the DC (bias) circuit equation for bias dependent small-signal analysis. These nonlinear equations are solved using a nonlinear equation solver *HYBRID* [4]. The residue function from the nonlinear equations are computed by a subroutine named as *FCN_HB* for large-signal analysis or *FCN_R* for small-signal analysis. In subroutine *FCN_HB*, a set of lower-level subroutines are called to perform the Fourier transforms, the device simulations, and formulation of the HB equations. Similarly, routine *FCN_R* organizes the calculation of S-parameters and DC responses. Both *FCN_HB* and *FCN_R* are called by the *HYBRID* program iteratively until a solution to the nonlinear equations is reached.

For optimization, a routine named as *FDF* is iteratively called by the optimizer until an optimal solution is reached. Inside *FDF*, two routines are activated, one is *FDF_HB* when large-signal optimization is required; the other is *FDF_R* if small-signal optimization is required. The routines *FDF_HB* and *FDF_R* organize the calculation of all the error functions and their derivatives w.r.t. optimization variables.

V. EXAMPLES WITH ONE-PORT NONLINEAR DEVICES

The use of McCAE to simulate FET devices has been fairly discussed. See, for example, [5]. In this section we demonstrate two simple examples containing one-port nonlinear devices. The first is a simple diode example. The second contains two fictitious nonlinear devices, which are described by quadratic I-V relations.

A Diode Example

The circuit file of the diode example follows.

```
!  Example  diode.ckt
!  A simple diode example
!  Model used: User-defined one port model.
!
Expression
!  user created model parameters

        IS:  1MA;  VB: 0.8;

!  file "diode.inc" contains all formulas of the diode model

#include "diode.inc"
end

Model

   RES  1  2    R=2;
   RES  3  4    R=2;

!  nonlinear diode model

   ONEPORT  3 2
        I:  I_MODEL     Q:    Q_MODEL;

    2POR  1  4;
end

Sweep
! HB simulation

  FREQ: 1GHZ  PIN: from 0DBM to 20DBM step=2DBM VG: 0 VD: 0;

! DC IV simulation

  VG: 0  VD: from -15 to 10 step=0.4;
end
```

The diode is described in the following include file:

```
!   File: diode.inc
!   A simple example of user-defined diode
!
!   List of model parameters:
!
!      IS  VB
!
!   List of current and charge computed from the model:
!
!      I_MODEL   Q_MODEL
!
!   Example of usage in the MODEL block:
!
!      ONEPORT  @node1  @node2  I: I_MODEL Q: Q_MODEL;
!
     AA = VDS_T/VB;
     BB = POS(AA - 40);
     CC = 40 * BB + (1 - BB) * AA;
     I_MODEL = IS * (EXP(CC) - 1);
     Q_MODEL = 0;

!************************  END OF MODEL ************************
```

The circuit is excited by a sinusoidal source. At the output port the current flows only in one direction, i.e., half of the sinusoidal waveform is truncated by the diode. The voltage waveform at the output port is shown in Fig. 3.

A Quadratically Nonlinear Circuit Example

In this example, we define two fictitious quadratically nonlinear devices. Using these two devices, a simple circuit example was created to monitor the numerical process of McCAE during program development. It is interesting to note that the output of this simple circuit approaches that of an ideal frequency doubler. The circuit file of the example follows.

```
! File: fiction.ckt
! A fictitious circuit with 2 quadratically nonlinear devices
! The response of this simple circuit is similar to
! that of a frequency doubler

expression
  a1 = vds_t * vds_t * 1.0E-5;
  a2 = 0.5 * a1;
```

```
end
model
  res  1 2  r=10;
  res  3 4  r=15;
  res  1 5  r=20;
  res  6 4  r=35;

  res  1 7  r=50;
  res  4 8  r=50;

  oneport 2 3 i=a1;
  oneport 5 6 i=a2;

  2biasport   7 0  8 0;
  2por        1   4;
end
sweep
   freq: 1ghz harm=4 pin: from 0dbm to 50dbm step=10dbm vg: 0  vd: 0;
end
```

After harmonic balance simulation, we plot the spectrum of the output voltage when the available input power is 30dBm. As shown in Fig. 4, the second harmonic component is the most significant one in the spectrum. The input signal is at frequency 1GHz. The output signal is at frequency 2GHz.

VI. EXAMPLES OF SMALL-SIGNAL SIMULATION AND OPTIMIZATION

Comparison of McCAE with Touchstone

We perform a small-signal analysis of a distributed amplifier. The circuit schematic, shown in Fig. 5, is based on the work of Ariel et al. [6]. The circuit contains 3 FET devices. We have used McCAE to compute the small-signal S-parameters of the distributed amplifier. The same example was simulated by Touchstone [7] and corresponding S-parameters were generated. The S-parameters from the two simulators are compared in Figs. 6 and 7. Fig. 6 displays the magnitude comparison and Fig. 7 the phase comparison. The discretely located circles, triangles, rectangles and diamonds represent Touchstone results. The continuous curves represent McCAE simulation. It is shown that the results from McCAE and Touchstone are virtually identical. This example confirms the accuracy of McCAE simulation.

The McCAE circuit file follows.

```
!   File: amp3_mc.ckt
!   Distributed amplifier with 3 FETs
!   This example is used to compare simulation results of McCAE and
!   Touchstone
!   The corresponding Touchstone circuit file is "amp3_tc.ckt"

Expression
!   FET intrinsic parameters
    T=3E-3;
    F=100000;
    CGS=.2E-3;
    GGS=.00001;
    RI=0.0001;
    CDG=.02E-3;
    CDC=.0;
    CDS=.0;
    RDS=100000;

!  User-defined device equations to simulate Touchstone linear FET model

    QGS_MODEL  = CGS * VGS_T;
    QGD_MODEL  = CDG * (VGS_T - VDS_T);
    IDS_MODEL1 = .03 * VGS_TAU;
    IDS_MODEL2 = .04 * VGS_TAU;
    IDS_MODEL3 = .02 * VGS_TAU;

!   FET parasitic parameters

    PLG= 0.01;
    PRG= 5;
    PRD= 5;
    PLD= 0.01;
    PRS= 5;
    PLS= 0.01;
    PRDS= 400;
    PCX= 1.5E-3;
    PCDS= 0.06E-3;

!   circuit elements

    LDD=   0.2;
    LD=    0.5 ;
    LG=    0.5 ;
    CG=    .5E-3;
    CD=    .5E-3;
end
Model

!   FET in Section 1
```

```
SRL   101  111   R= PRG  L= PLG;
SRL   102  112   R= PRD  L= PLD;
SRL   103    0   R= PRS  L= PLS;
SRC   103  102   R= PRDS C= PCX;
CAP   103  102   C= PCDS;

FETU1 101 102 103 IDS=IDS_MODEL1 QGS=QGS_MODEL QGD=QGD_MODEL TAU = T;

! FET in Section 2

SRL   201  211   R= PRG  L= PLG;
SRL   202  212   R= PRD  L= PLD;
SRL   203    0   R= PRS  L= PLS;
SRC   203  202   R= PRDS C= PCX;
CAP   203  202   C= PCDS;

FETU1 201 202 203 IDS=IDS_MODEL2 QGS=QGS_MODEL QGD=QGD_MODEL TAU = T;

! FET in Section 3

SRL   301  311   R= PRG  L= PLG;
SRL   302  312   R= PRD  L= PLD;
SRL   303    0   R= PRS  L= PLS;
SRC   303  302   R= PRDS C= PCX;
CAP   303  302   C= PCDS;

FETU1 301 302 303 IDS=IDS_MODEL3 QGS=QGS_MODEL QGD=QGD_MODEL TAU = T;

! Elements connected to the gate nodes

SRL  800     111   R=.1   L= LG;
SRL  111     211   R=.1   L= LG;
SRL  211     230   R=.1   L= LG;
SRL  230     311   R=.1   L= LG;
SRL  311     804   R=10   L=20;
CAP  230       0   C= CG;

! Elements connected to the drain nodes

SRLC  901      0  R=100 L= 10  C= 1E-3;
SRL   901    902  R=.1  L= LD;
SRL   902    923  R=.1  L= LD;
SRL   923    903  R=.1  L= LD;
SRL   112    901  R=.1  L= LDD;
SRL   212    902  R=.1  L= LDD;
SRL   312    903  R=.1  L= LDD;
CAP   901      0  C= CD;
CAP   902      0  C= CD;
CAP   923      0  C= CD;
CAP   903      0  C= CD;

! Bias circuit
```

```
   SRL  903 904        R=.1  L= 12;
   SRL  4    904       R=.1  L= 12;
   CAP  4      0       C= 40E-3;
   CAP  904    0       C= 180E-3;
   RES  3    804       R=  10 ;
   CAP  804    0       C=  200E-3 ;

!  DC blocking capacitor

   CAP 1  800  C= 100E-3;
   CAP 2  903  C= 100E-3;

! Bias sources grounded for S-parameter simulation

   RES  3 0  R=0.001;
   RES  4 0  R=0.001;

   2POR   1  2  ;
end

Data
#include "amp3_tc.dat";
end

Sweep
  FREQ: from 5GHZ to 30GHZ step=1GHZ VG=0 VD=3 MS11 MS21 MS12 MS22;
  FREQ: from 5GHZ to 30GHZ step=1GHZ VG=0 VD=3 PS11 PS21 PS12 PS22;
end
```

The Touchstone circuit file follows.

```
!  File: amp3_tc.ckt
!  Distributed amplifier with 3 FETs
!  This example is used to compare simulation results of McCAE and
!  Touchstone
!  The corresponding McCAE circuit file is "amp3_mc.ckt"

DIM
   FREQ  GHZ
   CAP   NF
   IND   NH
   TIME  NS
VAR
!  FET intrinsic parameters
   B=3E-3
   C=100000
   D=.2E-3
   E=.00001
   P=0.0001
   Q=.02E-3
   R=.0
```

```
   S=.0
   W=100000

!  FET parasitic parameters

   PLG= 0.01
   PRG= 5
   PRD= 5
   PLD= 0.01
   PRS= 5
   PLS= 0.01
   PRDS= 400
   PCX= 1.5E-3
   PCDS= 0.06E-3

!  circuit elements

   LDD=   0.2
   LD=    0.5
   LG=    0.5
   CG=    .5E-3
   CD=    .5E-3
CKT
!  FET in Section 1

   SRL   101  111   R^ PRG   L^ PLG
   SRL   102  112   R^ PRD   L^ PLD
   SRL   103    0   R^ PRS   L^ PLS
   SRC   103  102   R^ PRDS  C^ PCX
   CAP   103  102   C^ PCDS

   FET 101 102 103 G=.03 T^B F^C CGS^D GGS^E RI^P CDG^Q CDC^R CDS^S RDS^W

!  FET in Section 2

   SRL   201  211   R^ PRG   L^ PLG
   SRL   202  212   R^ PRD   L^ PLD
   SRL   203    0   R^ PRS   L^ PLS
   SRC   203  202   R^ PRDS  C^ PCX
   CAP   203  202   C^ PCDS

   FET 201 202 203 G=.04 T^B F^C CGS^D GGS^E RI^P CDG^Q CDC^R CDS^S RDS^W

!  FET in Section 3

   SRL   301  311   R^ PRG   L^ PLG
   SRL   302  312   R^ PRD   L^ PLD
   SRL   303    0   R^ PRS   L^ PLS
   SRC   303  302   R^ PRDS  C^ PCX
   CAP   303  302   C^ PCDS

   FET 301 302 303 G=.02 T^B F^C CGS^D GGS^E RI^P CDG^Q CDC^R CDS^S RDS^W
```

```
!   Elements connected to the gate nodes

    SRL  800       111   R=.1    L^ LG
    SRL  111       211   R=.1    L^ LG
    SRL  211       230   R=.1    L^ LG
    SRL  230       311   R=.1    L^ LG
    SRL  311       804   R=10    L=20
    CAP  230         0   C^ CG

!   Elements connected to the drain nodes

    SRLC   901         0  R=100 L= 10   C= 1E-3
    SRL    901       902  R=.1  L^ LD
    SRL    902       923  R=.1  L^ LD
    SRL    923       903  R=.1  L^ LD
    SRL    112       901  R=.1  L^ LDD
    SRL    212       902  R=.1  L^ LDD
    SRL    312       903  R=.1  L^ LDD
    CAP    901         0  C^ CD
    CAP    902         0  C^ CD
    CAP    923         0  C^ CD
    CAP    903         0  C^ CD

!   Bias circuit

    SRL  903 904       R=.1  L= 12
    SRL  4   904       R=.1  L= 12
    CAP  4     0       C= 40E-3
    CAP  904   0       C= 180E-3
    RES  3   804       R=  10
    CAP  804   0       C=  200E-3

!   DC blocking capacitor

    CAP 1  800  C= 100E-3
    CAP 2  903  C= 100E-3

!   Bias sources grounded for S-parameter simulation

    RES  3 0  R=0.001
    RES  4 0  R=0.001

    DEF2P       1  2  DAMP
FREQ
  SWEEP 1 30 1
OUT
    DAMP MAG[S11]  GR1
    DAMP ANG[S11]  GR2
    DAMP MAG[S21]  GR1
    DAMP ANG[S21]  GR2
    DAMP MAG[S12]  GR1
```

```
   DAMP ANG[S12]  GR2
   DAMP MAG[S22]  GR1
   DAMP ANG[S22]  GR2

   DAMP S11  SC2
   DAMP S22  SC2
   DAMP S12  SC1
   DAMP S21  SC3
GRID
   RANGE 0 30  5
   GR1   0 4  .5
   GR2  -180  180 60
```

Optimization of the Distributed Amplifier

We applied optimization to the 3-FET distributed amplifier. The objective was to obtain a K/Ka-band amplifier [8]. The operating frequency range is 14-37GHz. We impose a -7dB specification on the magnitudes of S11 and S22 and a 7dB specification on the magnitude of S21. These specifications were applied to the circuit in the form of fictitious measurement data.

We allow the parameters in the three FETs to vary independently. We also allow most of the linear elements to be optimized. A l_2 optimizer was used. The S-parameter response of the optimized circuit is shown in Fig. 8. The circuit performance is quite satisfactory compared to the specifications imposed.

In the example we allow parameters in the user-defined device models to be optimized. This is done only to demonstrate circuit optimization with variables in both the linear and the nonlinear parts of the circuit. Practically, optimizing device models for design purposes is useful only when the model is physics based.

The circuit file after optimization follows.

```
!  Example  amp3_ss.ckt
!  Small-signal simulation and optimization of a
!  distributed amplifier with 3 FETs
!  Models used: User-defined model with linear expressions
Expression

!  intrinsic FET parameters

   CGS1: ? 0.0642869PF?; CDG1: ?0.00393868PF?;  GM1: ?0.205545?;
```

```
   CGS2: ? 0.0512089PF?; CDG2: ?0.00888252PF?;  GM2: ?0.202763?;
   CGS3: ? 0.194105PF?; CDG3: ?0.00348507PF?;  GM3: ?0.429009?;

!  User-defined device equations

   QGS_MODEL1 = CGS1 * VGS_T;
   QGD_MODEL1 = CDG1 * (VGS_T - VDS_T);
   IDS_MODEL1 = GM1  * VGS_TAU;

   QGS_MODEL2 = CGS2 * VGS_T;
   QGD_MODEL2 = CDG2 * (VGS_T - VDS_T);
   IDS_MODEL2 = GM2  * VGS_TAU;

   QGS_MODEL3 = CGS3 * VGS_T;
   QGD_MODEL3 = CDG3 * (VGS_T - VDS_T);
   IDS_MODEL3 = GM3  * VGS_TAU;

!  FET parasitic parameters

   P_LG: 0.001NH;  P_RG: 5;      P_RD: 5;
   P_LD: 0.001NH;  P_RS: 0.001;  P_LS: 0.001NH;
   P_RDS: 400;     P_CDS: 0.06PF;

!  circuit elements

   LDD1: ?0.256217NH?;  LDD2: ?0.127622NH?; LDD3: ?0.18166NH?;
   LD1:  ?5.06176NH?;  LD2:  ?0.206252NH?; LD3:  ?3.69387NH?;
   LG1:  ?0.0209437NH?;  LG2:  ?0.370351NH?; LG3:  ?0.461399NH?;
   CG:   ?0.058704PF?;
   CD1:  ?0.041422PF?;  CD2:  ?0.102718PF?; CD3:  ?0.0189324PF?;
   CD4:  ?0.0103464PF?;

!  output responses

   MS11_DB = 10 * LOG10(MS11);
   MS22_DB = 10 * LOG10(MS22);
   MS21_DB = 10 * LOG10(MS21);
   MS12_DB = 10 * LOG10(MS12);
end

Model

!  FET in Section 1

   SRL  @gg1  @gate1   R: P_RG  L: P_LG;
   SRL  @dd1  @drain1  R: P_RD  L: P_LD;
   SRL  @ss1  @ground  R: P_RS  L: P_LS;
   RES  @ss1  @dd1     R: P_RDS;
   CAP  @ss1  @dd1     C: P_CDS;

   FETU1   @gg1 @dd1 @ss1
           IDS=IDS_MODEL1 QGS=QGS_MODEL1 QGD=QGD_MODEL1 TAU = 1PS;
```

```
!   FET in Section 2

    SRL  @gg2  @gate2   R: P_RG  L: P_LG;
    SRL  @dd2  @drain2  R: P_RD  L: P_LD;
    SRL  @ss2  @ground  R: P_RS  L: P_LS;
    RES  @ss2  @dd2     R: P_RDS;
    CAP  @ss2  @dd2     C: P_CDS;

    FETU1    @gg2 @dd2 @ss2
             IDS=IDS_MODEL2 QGS=QGS_MODEL2 QGD=QGD_MODEL2 TAU = 1PS;

!   FET in Section 3

    SRL  @gg3  @gate3   R: P_RG  L: P_LG;
    SRL  @dd3  @drain3  R: P_RD  L: P_LD;
    SRL  @ss3  @ground  R: P_RS  L: P_LS;
    RES  @ss3  @dd3     R: P_RDS;
    CAP  @ss3  @dd3     C: P_CDS;

    FETU1    @gg3 @dd3 @ss3
             IDS=IDS_MODEL3 QGS=QGS_MODEL3 QGD=QGD_MODEL3 TAU = 1PS;

!   Elements connected to the gate nodes

    SRL  @g0          @gate1   L: LG1  R: .01;
    SRL  @gate1       @gate2   L: LG2  R: .01;
    SRL  @gate2       @gate23  L: LG3  R: .01;
    SRL  @gate23      @gate3   L: LG3  R: .01;
    SRL  @gate3       @g4      L: ?6.83478NH?  R: ?5.9393?;
    CAP  @gate23      @ground  C: CG;

!   Elements connected to the drain nodes

    SRLC @d1          @ground  L: ?8.84243NH? R: ?121.53?  C:?10.0132PF?;
    SRL  @d1          @d2      L: LD1  R: 0.01;
    SRL  @d2          @d23     L: LD2  R: 0.01;
    SRL  @d23         @d3      L: LD3  R: 0.01;
    SRL  @drain1      @d1      L: LDD1 R: 0.01;
    SRL  @drain2      @d2      L: LDD2 R: 0.01;
    SRL  @drain3      @d3      L: LDD3 R: 0.01;
    CAP  @d1          @ground  C: CD1;
    CAP  @d2          @ground  C: CD2;
    CAP  @d23         @ground  C: CD3;
    CAP  @d3          @ground  C: CD4;

!   Bias circuit

    SRL  @d3          @d4      L: 12NH  R: .01;
    SRL  @drain_bias  @d4      L: 12NH  R: .01;
    CAP  @drain_bias  @ground  C: 40PF;
    CAP  @d4          @ground  C: 180PF;
```

```
   RES  @gate_bias  @g4      R: ?0.213765?;
   CAP  @g4         @ground  C: ?255.584PF?;

!  DC blocking capacitor

   CAP @input  @g0  C: 200PF;
   CAP @output @d3  C: 200PF;

   2BIASPORT  @gate_bias @ground  @drain_bias @ground;
   2POR       @input     @output;
end

Data
#include "amp3spec.dat"
end

Sweep
! S-parameter simulation

  FREQ: from 5GHZ to 45GHZ step=1GHZ VG: 0 VD: 3 MS11_DB MS22_DB MS21_DB;
end

Specification
  FREQ: from 14GHZ to 16GHZ step=1GHZ VG: 0 VD: 3 MS11_DB MS22_DB;
  FREQ: from 27GHZ to 37GHZ step=2GHZ VG: 0 VD: 3 MS11_DB MS22_DB MS21_DB;
end
```

VII. EXAMPLES OF LARGE-SIGNAL SIMULATION AND OPTIMIZATION

We consider the distributed amplifier circuit used in the previous section and shown in Fig. 5. Instead of using user-defined linear FET models, we use a large-signal Raytheon FET model. The model parameters for the 3 FETs are different. The circuit was simulated at fundamental frequencies 2GHz and 10GHz. The power gain and power added efficiency (PAE) of the circuit at the two frequencies are shown in Figs. 9 and 10, respectively. Our specifications include a 10dB lower specification on gain and a 15dB lower specification on power added efficiency. Both specifications must be satisfied when the available input power is swept from 5dBm to 10dBm. From Fig. 10 it can be seen that the circuit violates these specifications.

A minimax optimization was performed. In the first iteration, the objective function was 8.7. After 29 iterations, the objective function was reduced to -0.75. All specifications were satisfied. The gain and power added efficiency after optimization at 2GHz (10GHz) are shown in Fig. 11 (Fig. 12).

It should be noted that this is a very intensive optimization example. There are 30 optimization variables. In each iteration of the optimization, the HB equations have to be solved 4 times (at 2 fundamental frequencies and 2 input power levels). Each HB simulation is applied to a 3-FET nonlinear circuit. The total CPU time for optimization on an Apollo DN3500 was 2 hours and 20 seconds.

In the example we allow parameters in the nonlinear models to be optimized. This is done only to demonstrate circuit optimization with variables in both the linear and nonlinear parts of the circuit. Practically, optimizing nonlinear devices for design purposes is useful only when the device model is physics based.

The circuit file after optimization follows.

```
!  Example  amp3_hb.ckt
!  HB simulation and optimization of a
!  distributed amplifier with 3 FETs
!  Model used: Raytheon Model
!
Expression

!  intrinsic FET parameters

   CGS_1: ?0.164482PF?; FC_1: ?0.523419?; CGD_1: ?0.0151232PF?;
   CGS_2: ?0.15993PF?; FC_2: ?0.519134?; CGD_2: ?0.0168413PF?;
   CGS_3: ?0.120088PF?; FC_3: ?0.515132?; CGD_3: ?0.0173999PF?;

!  FET parasitic parameters

   P_LG: 0.01NH;     P_RG: 5;      P_RD: 5;
   P_LD: 0.01NH;     P_RS: 0.1;    P_LS: 0.001NH;
   P_RDS: 400;       P_CX: 1.5PF; P_CDS: 0.06PF;

!  circuit elements

   LDD1: ?0.700888NH?;  LDD2: ?0.689859NH?;  LDD3: ?0.830969NH?;
   LD1:  ?2.09739NH?;  LD2:  ?0.235692NH?;  LD3:  ?0.277101NH?;
   LG1:  ?0.356106NH?;  LG2:  ?0.620133NH?;  LG3:  ?0.368059NH?;
```

```
   CG:    ?0.067962PF?;
   CD1:  ?0.0646398PF?;  CD2:  ?0.128094PF?; CD3:  ?0.144516PF?;
   CD4:  ?0.14269PF?;

!  output responses

   GAIN_DB = POUT1 - PIN;
   PAE = (POUTW1 - PINW) / (ID0 * VD ) * 100;
   MS21_HB = SQRT(POUTW1/PINW);
end

Model

!  FET in Section 1

   SRL  @gg1  @gate1   R: P_RG  L: P_LG;
   SRL  @dd1  @drain1  R: P_RD  L: P_LD;
   SRL  @ss1  @ground  R: P_RS  L: P_LS;
   SRC  @ss1  @dd1     R: P_RDS C: P_CX;
   CAP  @ss1  @dd1     C: P_CDS;

   FETR   @gg1 @dd1 @ss1
        CGS0: CGS_1  CGD0: CGD_1  FC:   FC_1
        ALPHA: 1.9      BETA: 0.019  VT0: -2    THETA: 0.0035
        LAMBDA: 0.002   TAU: 3PS     IS: 5E-15  N: 1
        GMIN:  1.0E-07  VBI: 0.8     VBR: 20.0;

!  FET in Section 2

   SRL  @gg2  @gate2   R: P_RG  L: P_LG;
   SRL  @dd2  @drain2  R: P_RD  L: P_LD;
   SRL  @ss2  @ground  R: P_RS  L: P_LS;
   SRC  @ss2  @dd2     R: P_RDS C: P_CX;
   CAP  @ss2  @dd2     C: P_CDS;

   FETR   @gg2 @dd2 @ss2
        CGS0: CGS_2  CGD0: CGD_2  FC:   FC_2
        ALPHA: 1.9      BETA: 0.019  VT0: -2    THETA: 0.0035
        LAMBDA: 0.002   TAU: 3PS     IS: 5E-15  N: 1
        GMIN:  1.0E-07  VBI: 0.8     VBR: 20.0;

!  FET in Section 3

   SRL  @gg3  @gate3   R: P_RG  L: P_LG;
   SRL  @dd3  @drain3  R: P_RD  L: P_LD;
   SRL  @ss3  @ground  R: P_RS  L: P_LS;
   SRC  @ss3  @dd3     R: P_RDS C: P_CX;
   CAP  @ss3  @dd3     C: P_CDS;

   FETR   @gg3 @dd3 @ss3
        CGS0: CGS_3  CGD0: CGD_3  FC:   FC_3
        ALPHA: 1.9      BETA: 0.019  VT0: -2    THETA: 0.0035
```

```
      LAMBDA: 0.002   TAU: 3PS      IS: 5E-15  N: 1
      GMIN:  1.0E-07  VBI: 0.8      VBR: 20.0;

!  Elements connected to the gate nodes

   SRL  @g0         @gate1    L: LG1  R: .1;
   SRL  @gate1      @gate2    L: LG2  R: .1;
   SRL  @gate2      @gate23   L: LG3  R: .1;
   SRL  @gate23     @gate3    L: LG3  R: .1;
   SRL  @gate3      @g4       L: ?12.6431NH?  R: ?7.12846?;
   CAP  @gate23     @ground   C: CG;

!  Elements connected to the drain nodes

   SRLC @d1        @ground  L: ?32.4999NH? R: ?58.1039?  C:?1.52742PF?;
   SRL  @d1         @d2       L: LD1  R: 0.1;
   SRL  @d2         @d23      L: LD2  R: 0.1;
   SRL  @d23        @d3       L: LD3  R: 0.1;
   SRL  @drain1     @d1       L: LDD1 R: 0.1;
   SRL  @drain2     @d2       L: LDD2 R: 0.1;
   SRL  @drain3     @d3       L: LDD3 R: 0.1;
   CAP  @d1         @ground   C: CD1;
   CAP  @d2         @ground   C: CD2;
   CAP  @d23        @ground   C: CD3;
   CAP  @d3         @ground   C: CD4;

!  Bias circuit

   SRL  @d3         @d4       L: 12NH  R: .1;
   SRL  @drain_bias @d4       L: 12NH  R: .1;
   CAP  @drain_bias @ground   C: 40PF;
   CAP  @d4         @ground   C: 180PF;
   RES  @gate_bias  @g4       R: ?7.31688?;
   CAP  @g4         @ground   C: ?497.922PF?;

!  DC blocking capacitor

   CAP @input  @g0  C: 200PF;
   CAP @output @d3  C: 200PF;

   2BIASPORT  @gate_bias @ground  @drain_bias @ground;
   2POR       @input     @output;
end

Sweep
! S-parameter simulation

  FREQ: 2GHZ 10GHZ  VG: -.5 VD: 3;

! HB simulation

  FREQ: 2GHZ 10GHZ PIN: from -10DBM to  5DBM step= 5DBM
```

```
                              from   6DBM to  9DBM step= 1DBM
                              from  10DBM to 15DBM step=.5DBM
       VG: -.5  VD: 3 PAE  GAIN_DB;

     FREQ: 2GHZ 10GHZ PIN: from -50DBM to  0DBM step=10DBM
       VG: -.5  VD: 3 MS21_HB;
   end

   Specification
      FREQ: 2GHZ 10GHZ PIN: 5DBM 10DBM VG: -.5 VD: 3
      PAE > 15 GAIN_DB > 10;
   end
```

We also checked the consistency of small-signal and large-signal simulations for this 3-FET circuit. For example, the magnitude of S21 at 2GHz computed from small-signal simulation was 11.6939. The same response computed from HB simulation was 11.69 when the input level was -50dBm.

VIII. CONCLUSIONS

This report describes a major step in the development of the McCAE system, namely the simulation of nonlinear circuits with a general topology in both the linear and nonlinear subcircuits. The program can accommodate in one circuit multiple devices, different device models and different device topologies. The features that are applicable to such a general circuit include DC/small-signal/large-signal simulation, and multi-circuit (multi-frequency, multi-bias, and multi-input level) based optimization.

In the present version of McCAE the circuit topology can be completely arbitrary except for two restrictions. The first is that McCAE does not permit direct connection of two intrinsic nonlinear models. For example, some linear elements (which could be parasitic elements of a FET) must be placed between two intrinsic FETs. The second is that the number of input/output ports must be 2 and the number of bias ports must 2. Future effort should be directed to allow an arbitrary number of bias and input/output ports, and to allow direct connection of nonlinear models.

REFERENCES

[1] J.W. Bandler, Q.J. Zhang and R. Biernacki, "A unified theory for frequency-domain simulation and sensitivity analysis of linear and nonlinear circuits", *IEEE Trans. Microwave Theory and Techniques*, vol. 36, 1988, pp. 1661-1669.

[2] J.W. Bandler, S.H. Chen, S. Ye and Q.J. Zhang, "Integrated model parameter extraction using large-scale optimization concepts", *IEEE Trans. Microwave Theory and Techniques*, vol. 36, 1988, pp. 1629-1638.

[3] J.W. Bandler, Q.J. Zhang, S. Ye and S.H. Chen, "Efficient large-signal FET parameter extraction using harmonics", *IEEE Trans. Microwave Theory Tech.*, vol. 37, 1989, pp. 2099-2108.

[4] *MINPACK*, Argonne National Laboratory, March, 1980.

[5] J.W. Bandler, R.M. Biernacki, S.H. Chen, J. Song, S. Ye and Q.J. Zhang, "Analytically unified DC/small-signal/large-signal circuit design", Department of Electrical and Computer Engineering, McMaster University, Hamilton, Canada, Report SOS-89-5-R, 1989.

[6] D. Ariel, T. Thibout and J.L. Lacombe, "A 1 to 18 GHZ high gain ultra-broadband amplifier with temperature compensation", *Microwave Journal*, vol. 32, No. 5, May 1989, pp. 251-262.

[7] *Touchstone*, EEsof Inc., Westlake Village, CA 91362.

[8] M.J. Schindler, J.P. Wendler, M.P. Zaitlin, M.E. Miller and J.R. Dormail, "A K/Ka band distributed power amplifier with capacitive drain coupling", *IEEE Trans. Microwave Theory Tech.*, vol. 36, 1988, pp. 1902-1907.

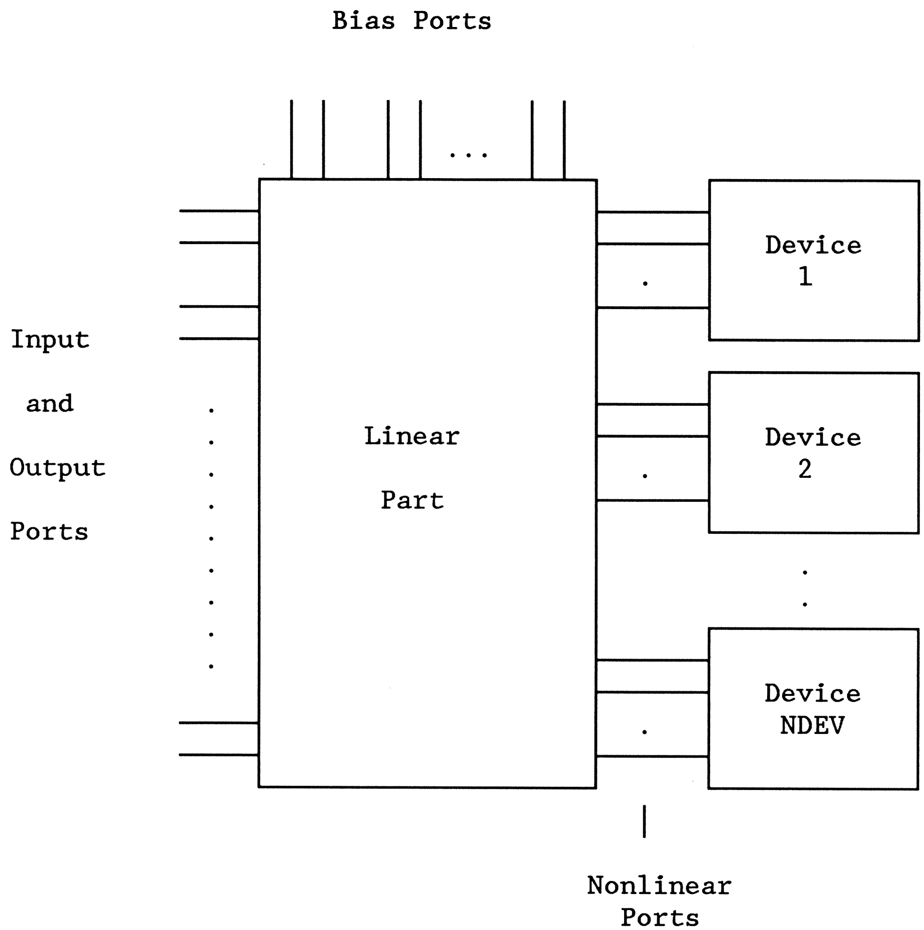

Fig. 1 A general circuit representation. The linear part may contain matching networks, bias circuits, etc. The total number of nonlinear devices is NDEV.

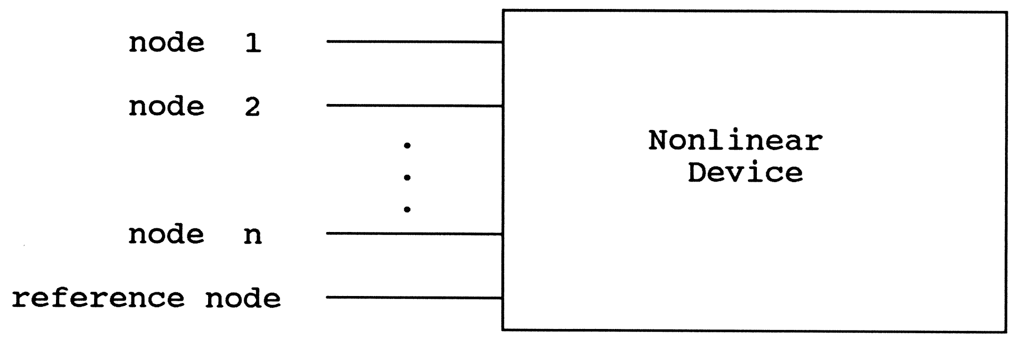

Fig. 2 A general representation of a nonlinear device. There are n+1 nodes. The last node is a reference node. The device is considered to be an n-port device. The ith port is between node i and the reference node, i = 1, 2, ..., n.

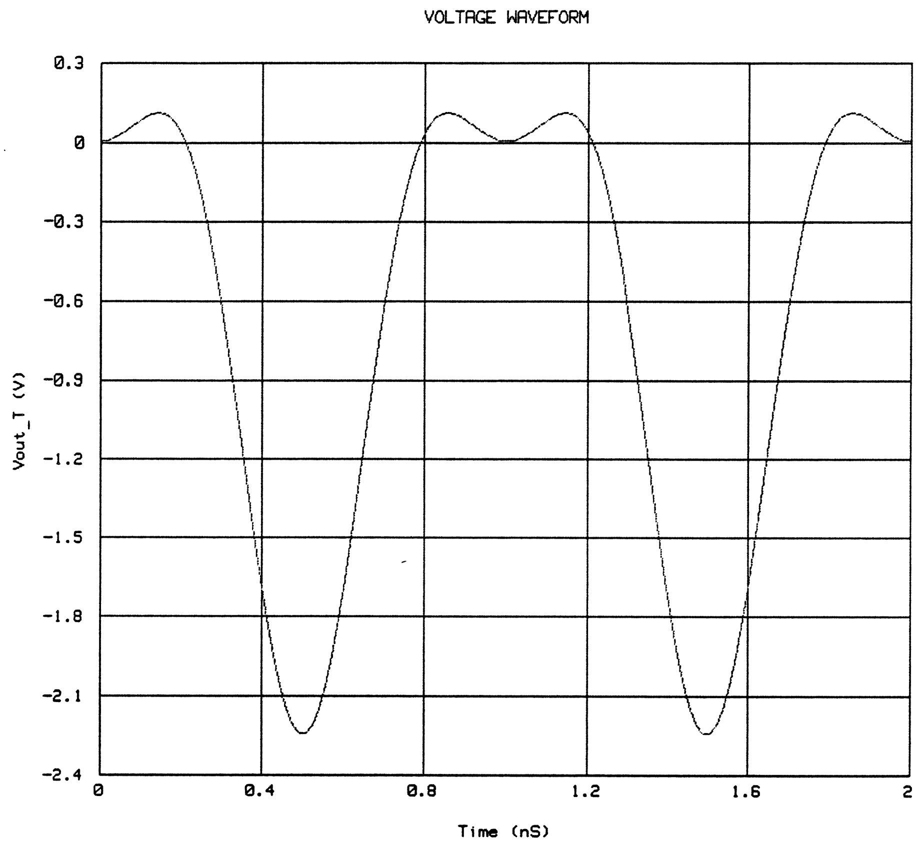

Fig. 3 Voltage waveform at the output port of the simple diode circuit. The positive half of the sinusoidal signal is truncated by the diode.

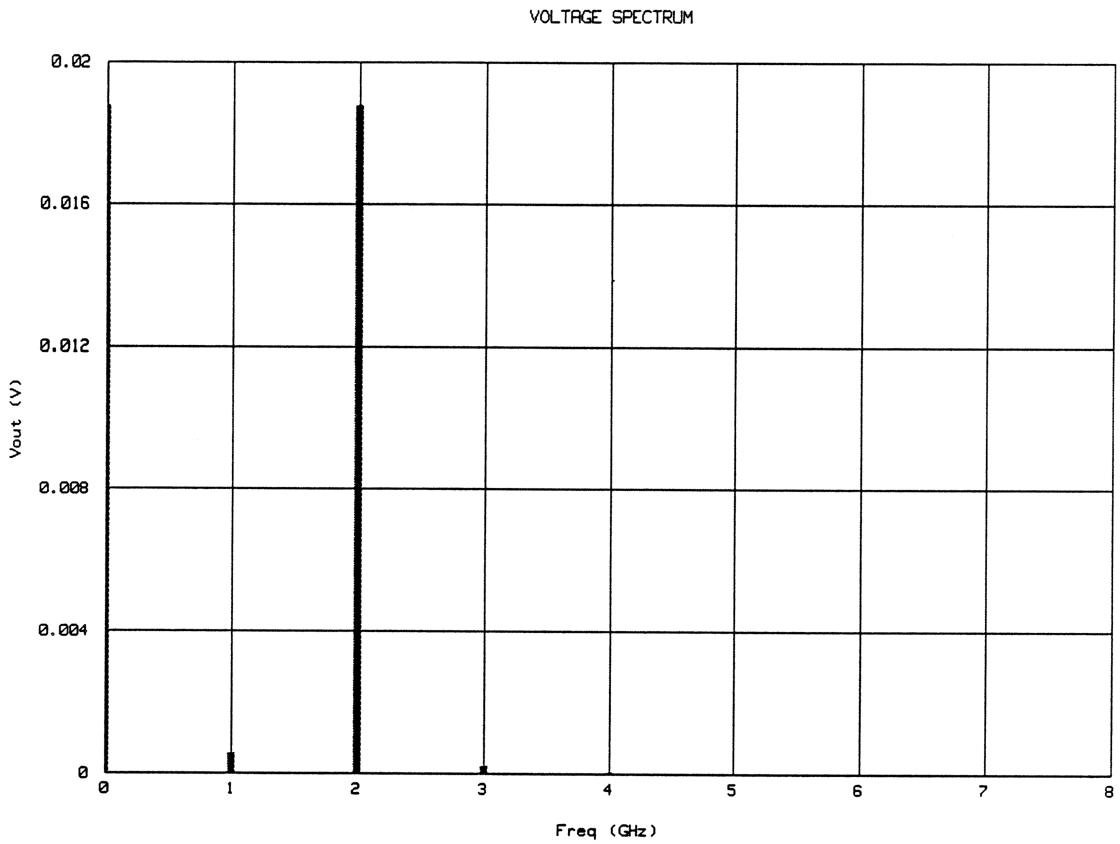

Fig. 4 Voltage spectrum at the output port of the quadratically nonlinear circuit. The input signal is at 1GHz. The output signal is at 2GHz. This circuit functions as a frequency doubler.

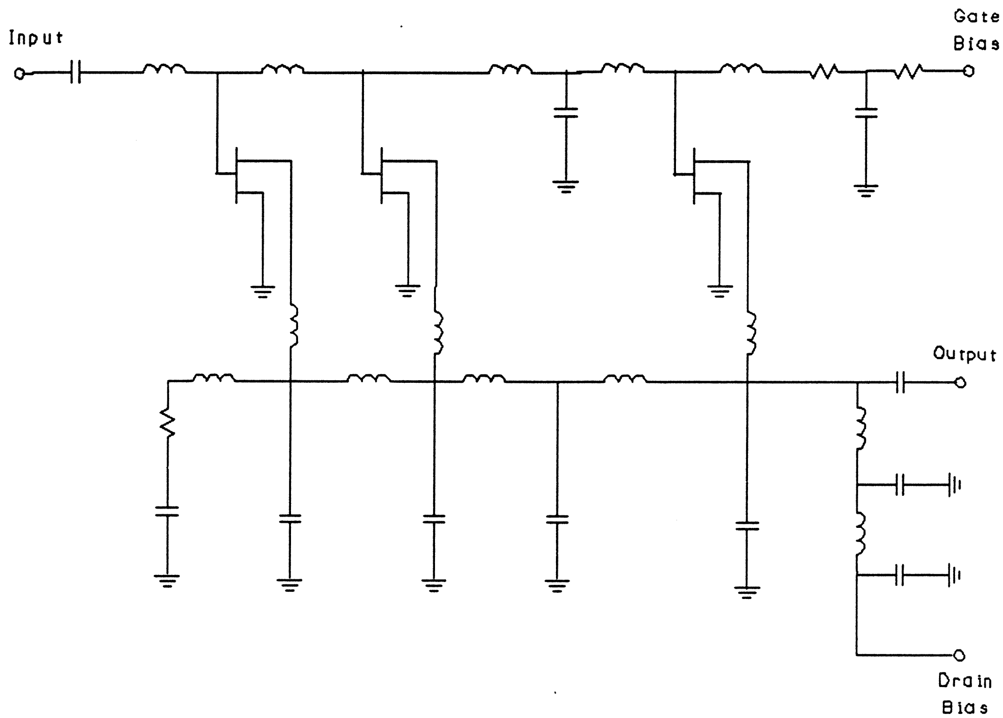

Fig. 5 Schematics of a distributed amplifier with 3 FETs.

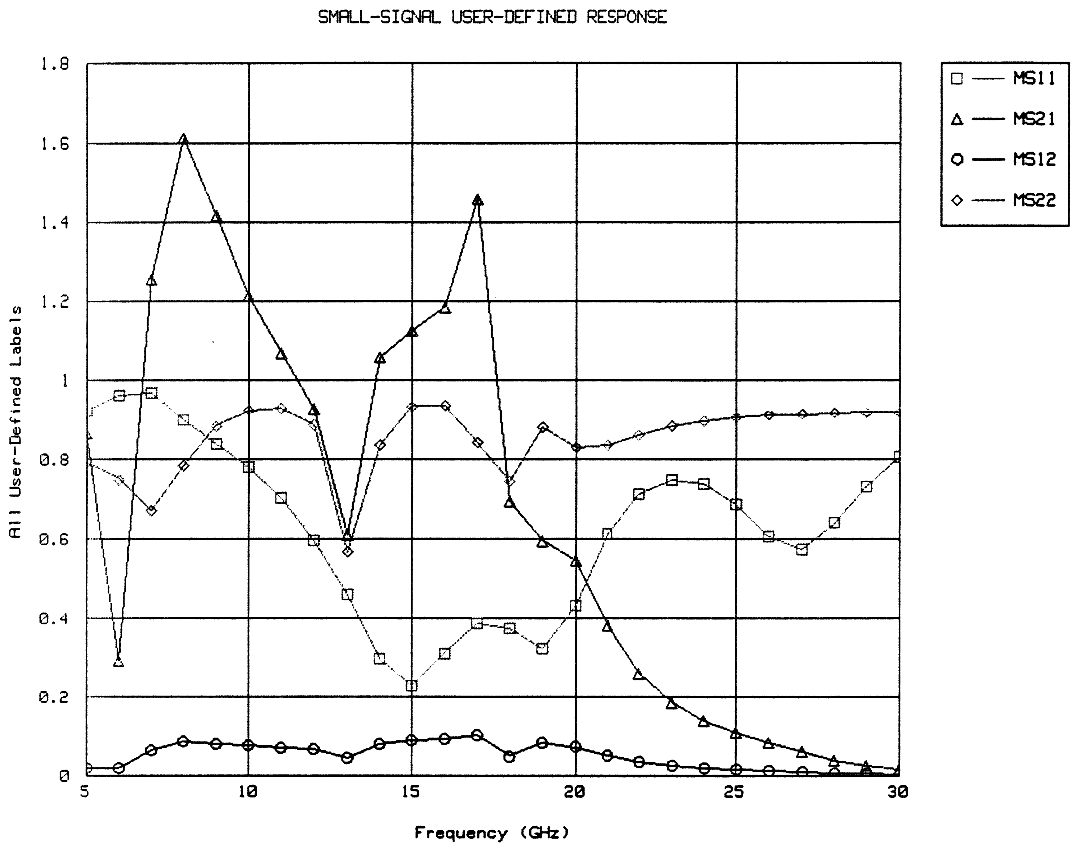

Fig. 6 Magnitude of S-parameters of a distributed amplifier with 3 FETs. The circles, triangles, rectangles and diamonds represent Touchstone results. The curves represent McCAE results. The results from both programs agree perfectly.

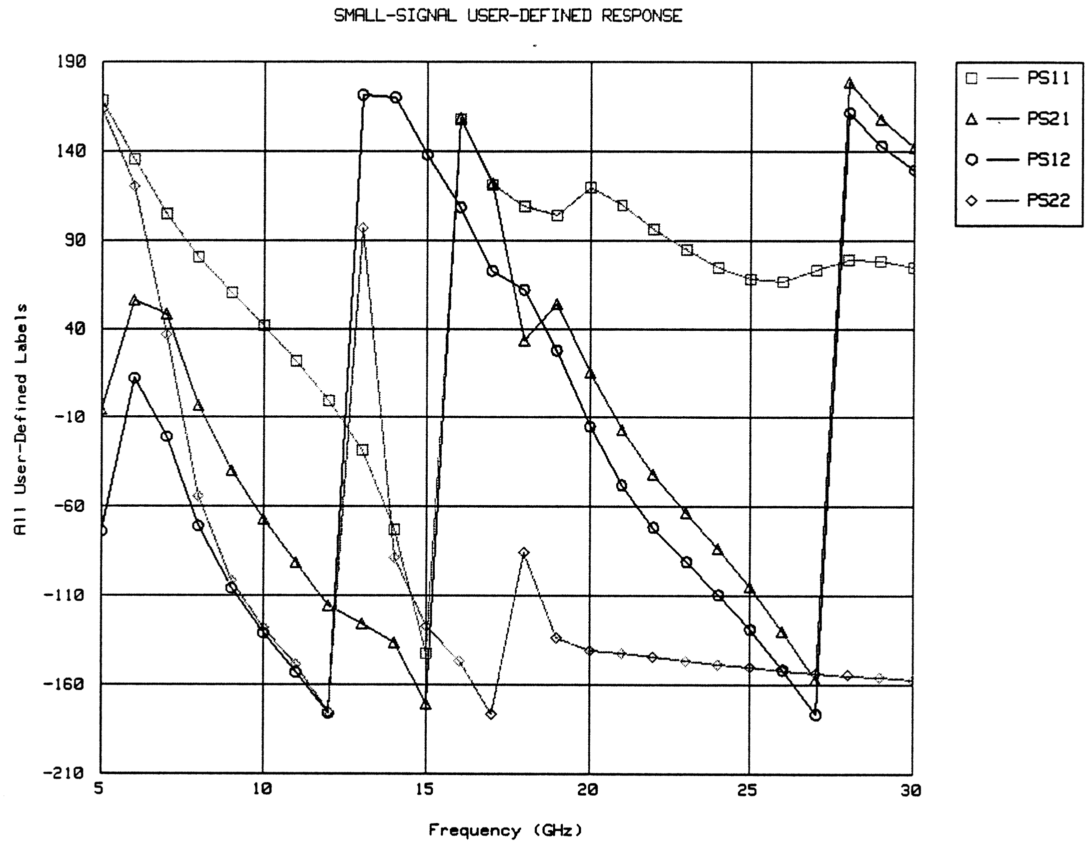

Fig. 7 Phase of S-parameters of a distributed amplifier with 3 FETs. The circles, triangles, rectangles and diamonds represent Touchstone results. The curves represent McCAE results. The results from both programs agree perfectly.

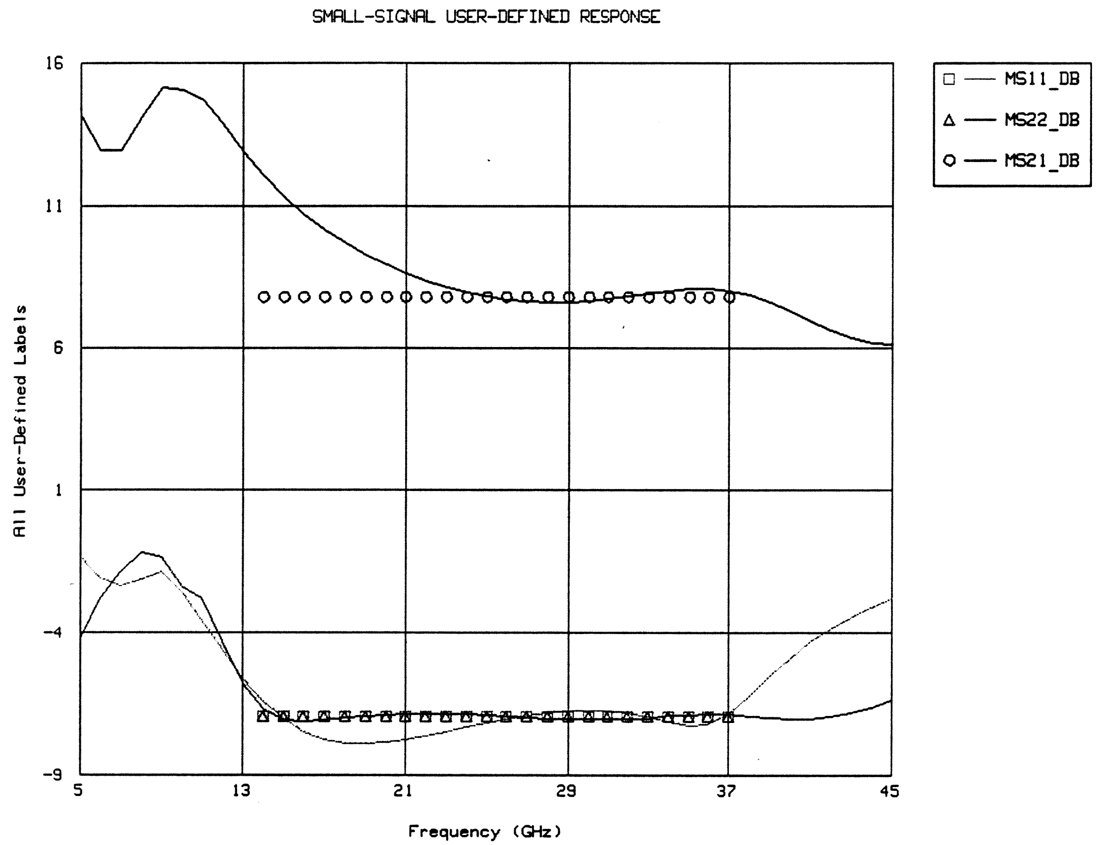

Fig. 8 Optimized S-parameter responses of the 3 FET distributed amplifier operating in the 14-37GHz frequency range. The specifications are -7dB on the magnitudes of S11 and S22, and 7dB on the magnitude of S21. The circuit was optimized by a l_2 optimizer.

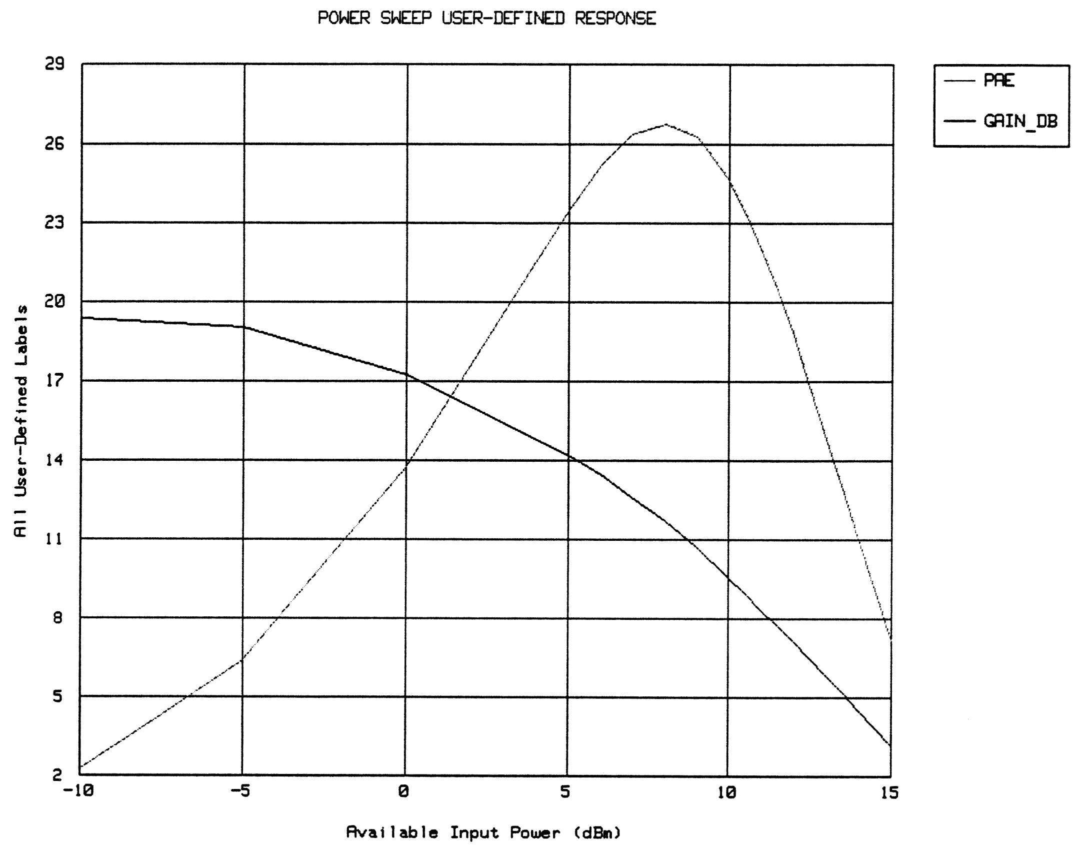

Fig. 9 Gain and Power Added Efficiency (PAE) of the distributed amplifier before optimization. The fundamental frequency is 2GHz.

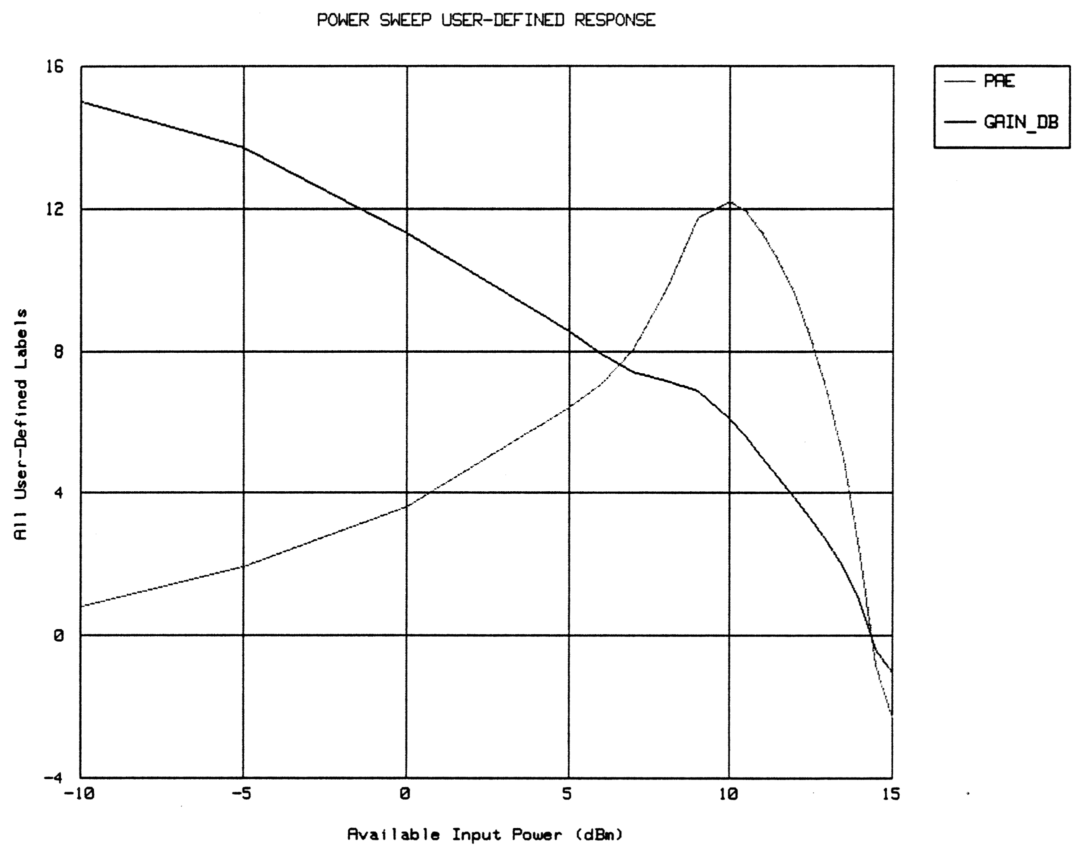

Fig. 10 Gain and Power Added Efficiency (PAE) of the distributed amplifier before optimization. The fundamental frequency is 10GHz.

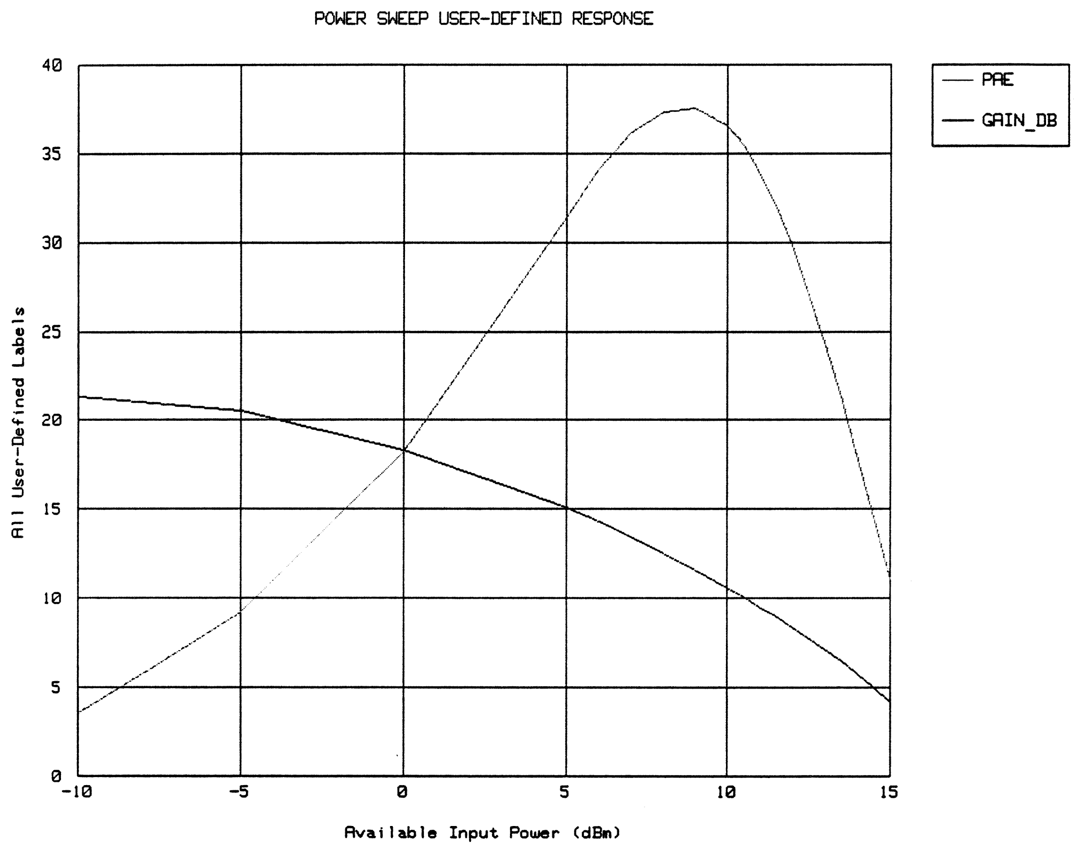

Fig. 11 Gain and Power Added Efficiency (PAE) of the distributed amplifier after optimization. The fundamental frequency is 2GHz.

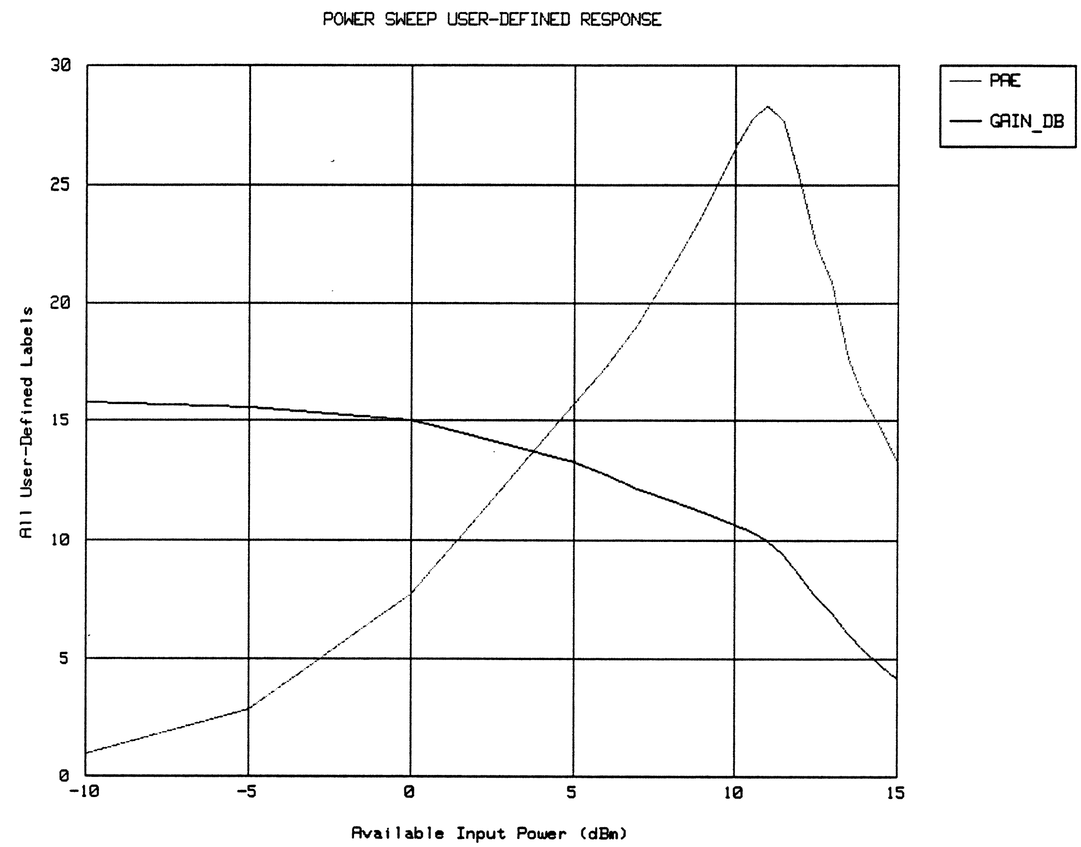

Fig. 12 Gain and Power Added Efficiency (PAE) of the distributed amplifier after optimization. The fundamental frequency is 10GHz.