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ABSTRACT

In this paper we present the compression analysis of a BJT high power amplifier circuit. This circuit was chosen by Microwave Engineering Europe (MEE) as a challenge to CAD programs. The bipolar transistor is modeled by a SPICE model. Extraction of the model parameters was performed by fitting the model responses to vendor-published S-parameter data. In addition to compression analysis of the amplifier we carried out Monte Carlo statistical simulation and sensitivity analysis. All simulations and optimizations were performed by our CAD software system OSA90/hope, in particular by our nonlinear harmonic balance simulator.

INTRODUCTION

The harmonic balance (HB) technique is an efficient method for nonlinear steady-state circuit analysis [1-3]. It has been widely applied to nonlinear analysis and design of microwave circuits such as amplifiers, mixers and frequency doublers [4-7]. However, HB analysis of high power amplifiers may be a challenge to HB solvers [8] since the strong nonlinearity of the circuits may cause problems such as non-convergence. The success of the simulation depends on the accuracy of models and the intelligent use of nonlinear HB simulators.

In September 1993, Microwave Engineering Europe initiated a nonlinear CAD benchmark for the most popular microwave commercial HB simulators. The problem was the nonlinear simulation of a high power BJT amplifier.

The amplifier was designed by Jennings and Perry for communication applications around 2 GHz with less than 1 W output power [8]. The amplifier worked well in practice but proved very difficult to simulate using nonlinear HB simulators.

The difficulty came from the characteristics of the transistor. It is a classic power BJT with a poor S_{12} (i.e., the device must be regarded as bilateral), an electrically large package, and an emitter ballast resistor. Therefore, the success of analyzing this circuit depends largely on the accuracy of the model for the transistor.

We used OSA90/hope [9] to investigate the performance of this amplifier. In this paper we present compression analysis of the amplifier. This includes model parameter extraction for the transistor, nonlinear harmonic balance (HB) simulations, statistical analysis and sensitivity analysis.

CIRCUIT STRUCTURE AND CHARACTERISTICS [8]

The schematic of the amplifier is shown in Fig. 1. It consists of a power BJT (Avantek AT64023) and a number of distributed elements. The BJT is biased for a DC collector current of 100 mA and a DC collector emitter voltage of 16 V. The distributed elements for input and output matching circuits are realized in microstrip on standard 1.5 mm FR4 board. The amplifier was designed to provide a high power driver to saturate other high power devices being tested under nonlinear operation.

The configuration of the amplifier results in a very narrow band response centered at 2 GHz with the power characteristics having been somewhat sacrificed in favour of good impedance and gain characteristics [8].

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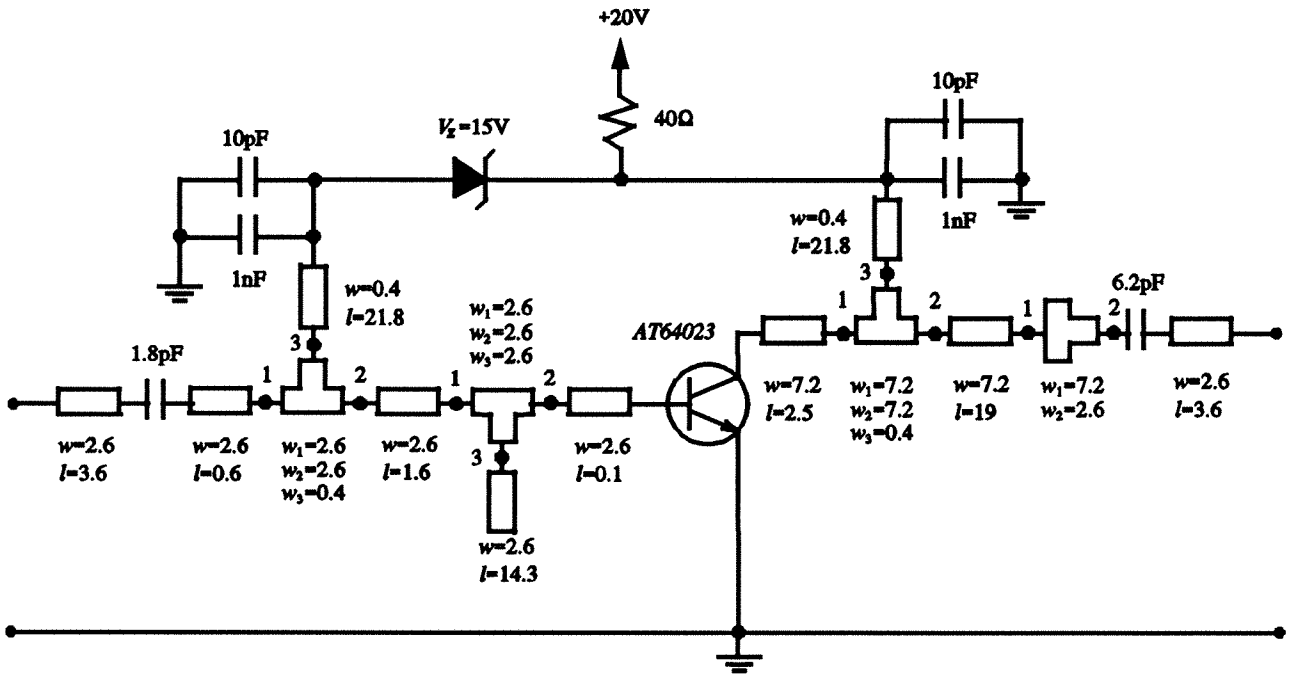


Fig. 1 The power amplifier circuit. Dimensions are in mm. The substrate thickness is 1.5 mm. The relative dielectric constant is 4.75. The metallization is 35 μm thick copper.

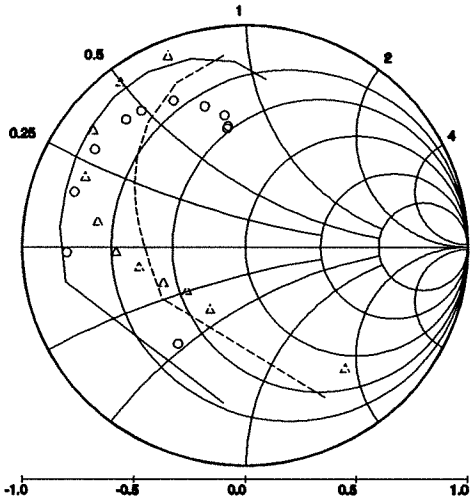
DEVICE MODELING

The model of the BJT used for simulation is the SPICE Gummel-Poon nonlinear model augmented by a diode circuit to model the distributed base capacitance and resistance, and a package model provided by Avantek [10]. OSA90/hope employs unified DC, small-signal and large-signal modeling. The small-signal model is derived, when necessary, from the nonlinear model. This ensures consistent responses from the DC, small-signal and HB analysis.

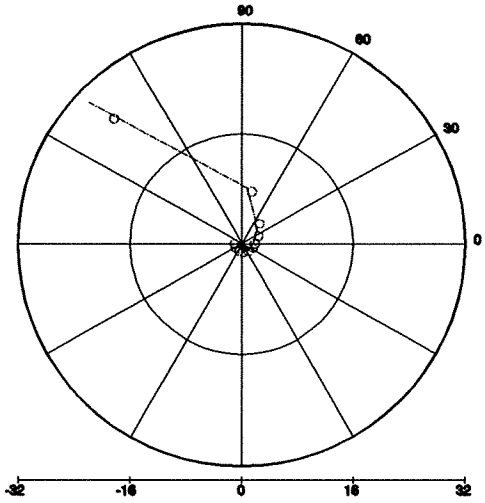
When the Gummel-Poon model with the parameters specified by Avantek [10] was applied to small-signal simulation, we noticed some discrepancies between the simulated S parameters and the average measured S-parameter data, also provided by Avantek [10]. The reason for such discrepancies can be attributed to the still fairly common "disjoint" modeling of small- and large-signal operation of the transistor.

Assuming that the S-parameter measurements are more reliable than the model provided by Avantek we performed model refinement for a better S-parameter fit. To this end we used the parameter extraction capabilities of OSA90/hope. Since the data represents the average values, the extracted model represents a typical device. If we wish to obtain the best model for the particular transistor used to build the amplifier, the S-parameter measurements for that transistor would be required.

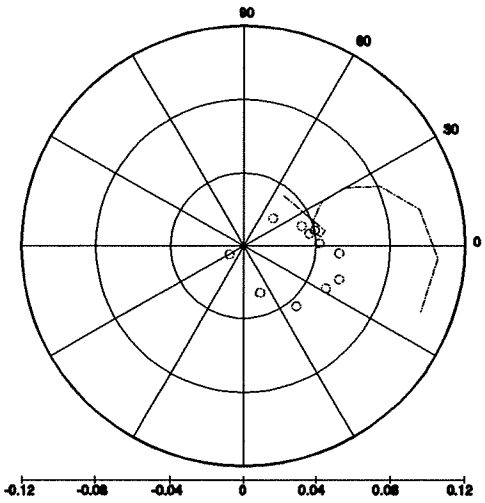
Fig. 2 shows the match between the measured and simulated S parameters using the model provided by Avantek. Fig. 3 shows the much improved match using the optimized model.



(a) S_{11} (model: ——, measured: o) and S_{22} (model: ---, measured: ▵).

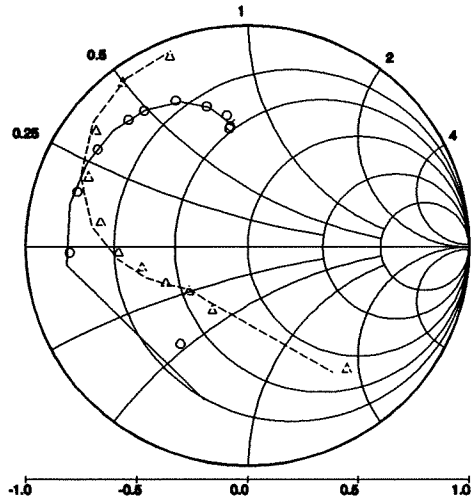


(b) S_{21} (model: ---, measured: o).

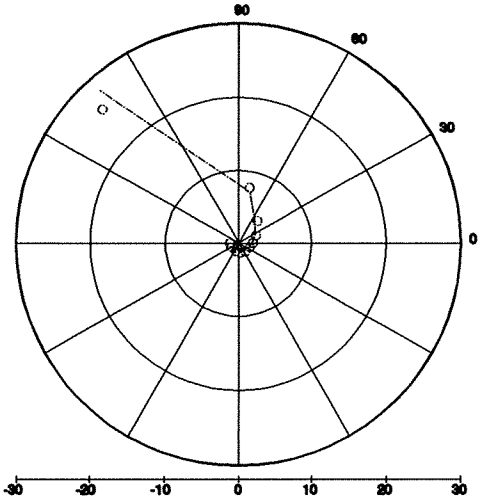


(c) S_{12} (model: ---, measured: o).

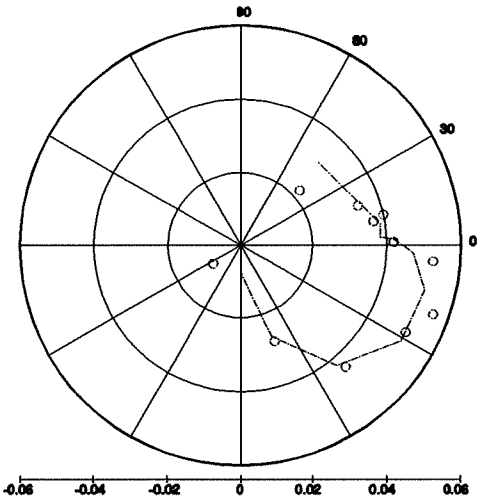
Fig. 2 S-parameter match between the model provided by Avantek and the typical (average) S parameters [10].



(a) S_{11} (model: ——, measured: o) and S_{22} (model: ---, measured: ▵).



(b) S_{21} (model: ---, measured: o).



(c) S_{12} (model: ---, measured: o).

Fig. 3 S-parameter match between the optimized model and the typical (average) S parameters [10].

SMALL- AND LARGE-SIGNAL SIMULATION

Using OSA90/hope, we performed both small-signal and large-signal HB simulations of the amplifier with the BJT model provided by Avantek and our optimized model extracted from the *S*-parameter data.

Small-signal gain of 16.3 dB and output power of 26.6 dBm at 1 dB gain compression, both at 2 GHz, were obtained using directly the model provided by Avantek. The corresponding results obtained using the optimized model were 10.7 dB small-signal gain and 23.4 dBm output power at 1 dB gain compression. The measured values at 2 GHz are: 12.2 dB small-signal gain and 23.0 dBm output power at 1 dB gain compression [8]. The simulation results using the optimized model are much closer to the measurements. The small-signal gain versus frequency and the output power versus input power of the amplifier are shown in Figs. 4 and 5, respectively.

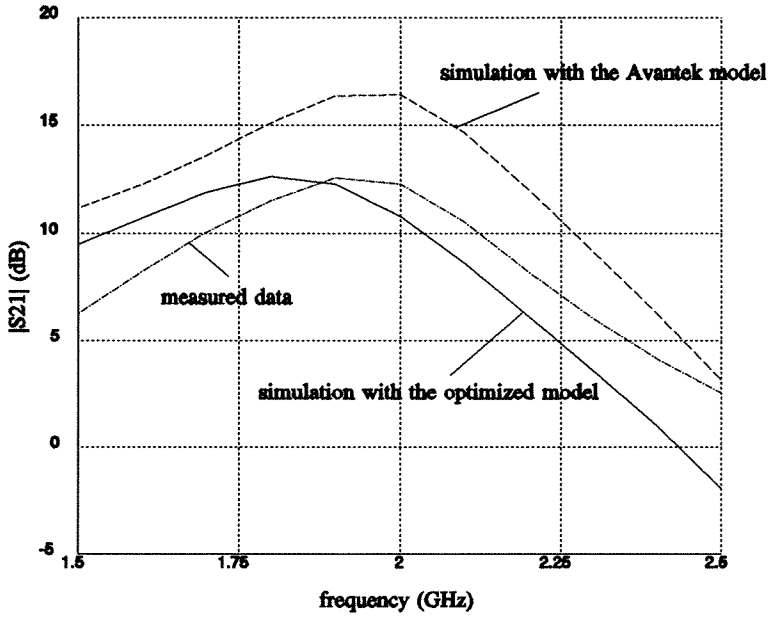


Fig. 4 Small-signal gain versus frequency of the amplifier.

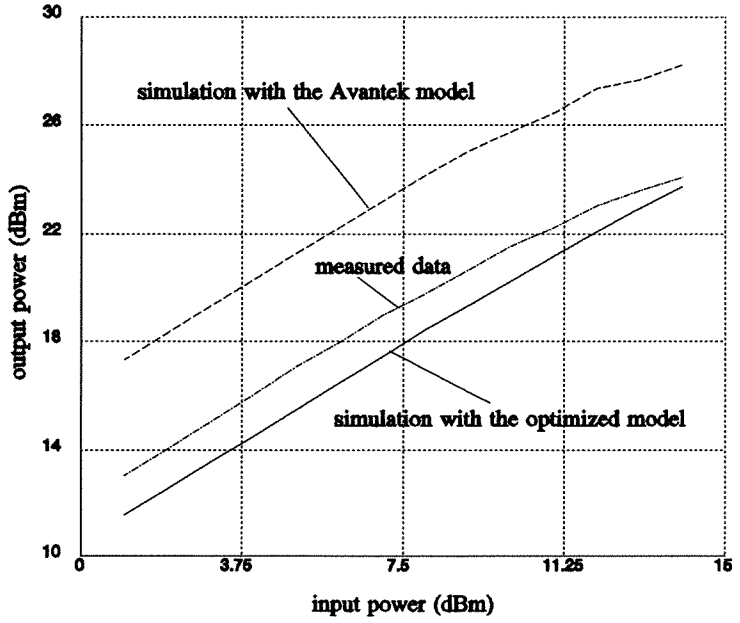


Fig. 5 Output power versus input power of the amplifier.

STATISTICAL ANALYSIS

The differences between the model provided by Avantek and the model obtained from the *S* parameters reveal the uncertainties associated with the device model. For an engineer to be confident with the design, a single simulation based on a single model may not be sufficient.

This motivated us to conduct statistical analysis of the amplifier to investigate the effect of parameter tolerances of the transistor model on the output power. The nominal parameter values were chosen as the average of the values provided by Avantek and the values of the optimized model. Tolerances were assigned to the model parameters according to the differences between the models. Monte Carlo simulation was carried out using 100 outcomes. The output power versus input power at 2 GHz is shown in Fig. 6.

The output power at 1 dB gain compression at 2 GHz are spread between 23.2 dBm and 27.2 dBm. This reflects the model uncertainty and is illustrated by the histogram shown in Fig. 7.

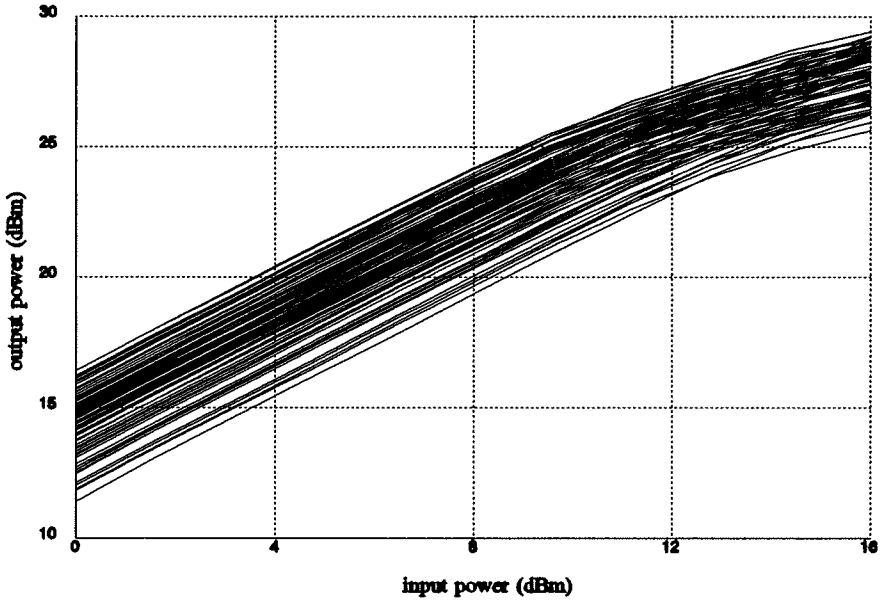


Fig. 6 Monte Carlo sweep of output power versus input power at 2 GHz.

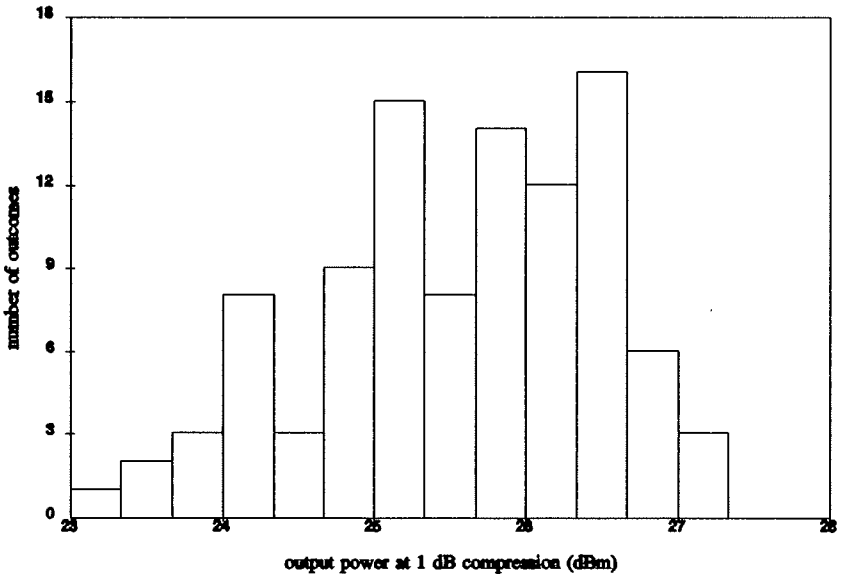


Fig. 7 Histogram of output power (dBm) at 1 dB gain compression at 2 GHz for assumed model uncertainty.

SENSITIVITY ANALYSIS

We have further investigated the sensitivity of the output power at 1 dB gain compression at 2 GHz w.r.t. the elements in the input and output matching circuits on a minimax design basis. The result shows that the response is more sensitive to the following parameters: the length of the open stub in the input matching circuit, the widths and lengths of the microstrip lines in the output matching circuits, than to the other parameters in the circuits.

CONCLUSIONS

We have presented the compression analysis of a high power BJT amplifier [8]. Parameter extraction was employed to refine the published Gummel-Poon model [10] of the transistor. Better agreement between our simulation results and the measurements of the amplifier has been obtained using the refined model rather than the Gummel-Poon model provided by Avantek. This exemplifies potential problems with vendor-supplied device models and a limited confidence the designer should have in such models. Different model implementations in different CAD packages and different parameter extraction procedures may contribute to this problem. It is more reliable to establish the model from measurements in a consistent manner within the same CAD environment. The statistical analysis by Monte Carlo simulation indicated that the BJT model accuracy is very important in the circuit simulation. Our sensitivity analysis identifies the circuit elements critical for the design.

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