COST-DRIVEN PHYSICS-BASED LARGE-SIGNAL SIMULTANEOUS DEVICE AND CIRCUIT DESIGN

J.W. Bandler, R.M. Biernacki, Q. Cai
and S.H. Chen

SOS-94-9-R

October 1994

(Revised January 1995)

COST-DRIVEN PHYSICS-BASED LARGE-SIGNAL
SIMULTANEOUS DEVICE AND CIRCUIT DESIGN

J.W. Bandler[*], R.M. Biernacki[*], Q. Cai and S.H. Chen[*]

Optimization Systems Associates Inc.
P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7

ABSTRACT

We present a cost-driven approach to the emerging demand for simultaneous device and circuit design. Here, an analytic physics-based Raytheon model facilitates fast large-signal simulation and optimization. A novel one-sided Huber approach is applied to design centering. The problem of cost-driven design is formulated as the minimization of the cost function while maintaining the required yield. Devices and matching circuits are optimized simultaneously, the advantages of which are demonstrated by a single-stage power amplifier design.

INTRODUCTION

Automated physics-based CAD directly links the physical parameters (geometrical, material, process) with performance and yield specifications in MMIC design. The potential advantages of optimization-driven physics-based CAD have been demonstrated in a number of publications, e.g., [1-4]. The advent of more powerful computers has increased the drive in using physical models and physics-based models for microwave CAD to meet the requirement of predictability and economization [5]. Space Mapping [6] will pave the way to automating the link between physics-based and physical simulations.

Statistical design centering (yield optimization) has been considered as indispensable for the design of MMICs where all the active and passive components are fabricated on a common semi-insulating substrate (e.g. [1-5]). Post-production tuning of MMICs is restricted, and device replacement is not possible. The production yield depends on parameters such as nominal values, tolerances and uncertainties. Yield optimization maximizes the yield by optimizing the nominal values of the design variables while keeping tolerances constant. However, the cost for obtaining such tolerances may be high. There is a trade-off between the yield and the cost. Therefore, cost-driven design is

* J.W. Bandler, R.M. Biernacki and S.H. Chen are also with the Simulation Optimization Systems Research Laboratory and Department of Electrical and Computer Engineering, McMaster University, Hamilton, Ontario, Canada L8S 4L7.

necessary for minimizing the cost while maintaining the required yield.

Device modeling is the basis for circuit simulation and optimization. A number of large-signal analytical physics-based GaAs MESFET models have been developed during the last decade, e.g., [7, 8]. Those models involve iterations to solve for an intermediate parameter v_1 which requires certain computational effort. Therefore, they are not efficient enough for cost-driven design when a large number of circuits have to be repeatedly simulated. To facilitate fast large-signal simulation and optimization we use the physics-based Raytheon (PBR) model [9] where the empirical parameters of the Raytheon model [10] are calculated from the physical parameters using analytical formulas. The PBR is implemented in conjunction with the built-in Raytheon model (FETR) of OSA90/hope [11].

We present, for the first time, a one-sided Huber approach [12] to physics-based design centering. The design centering problem is formulated using the one-sided Huber function to maximize design yield. The problem of cost-driven design is formulated as the minimization of the cost function [13] subject to a specified yield.

The advantages of our approach are demonstrated by a single-stage power amplifier design. The physical parameters of the device, such as FET gate length, channel thickness and doping density, and the elements of the matching circuits are optimized simultaneously.

Our approach is implemented in the CAD system OSA90/hope which is used to generate all the results presented in this paper.

PHYSICS-BASED RAYTHEON MODEL

In the Raytheon model [10] the drain current I_d of a FET is calculated by

$$I_d = \frac{\beta[v_{gs}(t-\tau)-V_{T0}]^2}{1-\theta[v_{gs}(t-\tau)-V_{T0}]}(1+\lambda v_{ds})P(\alpha, v_{ds}) \quad (1)$$

where

$$P(\alpha, v_{ds}) = \begin{cases} 1 - \left[1 - \frac{\alpha v_{ds}}{3}\right]^3 & \text{for } 0 < v_{ds} < \frac{3}{\alpha} \\ 1 & \text{for } v_{ds} \geq \frac{3}{\alpha} \end{cases} \quad (2)$$

α, β, λ, θ, τ and V_{T0} are empirical model parameters. To obtain the PBR model we calculate the empirical model parameters from the physical parameters using the analytical expressions derived by D'Agostino *et al.* [9]. The physical parameters of the PBR model include L the gate length, a the channel thickness, Z the gate width, E_s the electric field value at the electron drift velocity saturation, q the electron charge, μ_0 the low-field electron mobility, N_d the doping density, ε the dielectric permittivity and V_{bi} the built-in voltage.

Since analytical expressions are used in the computations of the PBR model it is very efficient for large-signal circuit simulation and optimization, particularly for cost-driven design. The accuracy of the PBR has been demonstrated in [9] by comparing the DC characteristics of the model with those of the measured data.

DESIGN CENTERING USING THE ONE-SIDED HUBER FUNCTION

In statistical design centering a number of statistical outcomes of circuit parameters, denoted by ϕ^i, are considered. In our physics-based design centering ϕ^i include the physical parameters of the devices and the parameters of the matching circuit elements. The design yield can be estimated as

$$Y = \frac{N_a}{N} \tag{3}$$

where N_a is the number of acceptable outcomes and N is the total number of outcomes considered.

Following the method of Bandler and Chen [13], for each outcome we create a generalized ℓ_p function $\nu(\phi^i)$ whose value is zero or negative if the outcome is acceptable. The design centering problem is then formulated as the minimization of the objective function $U(\phi^0)$ defined by [12]

$$U(\phi^0) = \sum_{i=1}^{N} \rho_k^+[\alpha_i \nu(\phi^i)] \tag{4}$$

where ϕ^0 is the vector of nominal circuit parameters to be centered, α_i is a positive multiplier associated with the ith outcome, ρ_k^+ is the one-sided Huber function defined by

$$\rho_k^+(f) = \begin{cases} 0 & \text{if } f \le 0 \\ f^2/2 & \text{if } 0 < f \le k \\ kf - k^2/2 & \text{if } f > k \end{cases} \tag{5}$$

and k is a positive constant threshold value (f is an error function which is $\alpha_i \nu(\phi^i)$ in our case).

FORMULATION OF COST-DRIVEN DESIGN

In Monte Carlo simulation a statistical outcome ϕ^i can be represented by

$$\phi^i = \phi^0 + \Delta\phi^i \tag{6}$$

where the random perturbation $\Delta\phi^i$ depends on the tolerances (standard deviations in normal distributions) of the parameter statistical distributions. Let

$$x = [x_1\ x_2\ ...\ x_m]^T \tag{7}$$

be the parameter tolerance vector where m is the total number of statistical variables. In the yield optimization problem x is kept constant while optimizing the parameter nominal value ϕ^0 to increase the yield. In the present implementation of cost-driven design ϕ^0 is kept constant and x is optimized to reduce the cost since the larger the parameter tolerances the lower the cost. We formulate the problem of cost-driven design as

$$\begin{array}{c} \text{minimize } C(x) \\ x \end{array} \tag{8}$$

$$\text{subject to } Y \ge Y_S$$

where Y is the design yield defined in (3), Y_S is the specified yield and $C(x)$ is the cost function. In our calculation we use the cost function defined by [13]

$$C(x) = \sum_{i=1}^{m} \frac{c_i}{x_i} \tag{9}$$

where c_i is a nonnegative weighting factor associated with the ith design variable.

A SINGLE-STAGE POWER AMPLIFIER DESIGN

As an example we consider a single-stage power amplifier shown in Fig. 1. The design is based on the circuit structure described in [11]. The amplifier is designed as Class-A. The design specifications are at 10 GHz frequency and 10 dBm input power

$$P_{out}[1] \ge 26 \text{ dBm}$$
$$P_{out}[2] \le 4 \text{ dBm}$$
$$PAE \ge 30 \text{ \%}$$

where $P_{out}[1]$ and $P_{out}[2]$ are the fundamental output power and the second harmonic output power, respectively, PAE is the power-added efficiency. We performed nominal design, yield optimization and cost-driven design using OSA90/hope. The gate length L, gate width Z, channel thickness a and the doping density N_d of the MESFET, the physical lengths of transmission lines TL_1 and TL_2 in the matching circuits are chosen as design variables. The following constraints are imposed on the design variables of the MESFET in order to guarantee that their values are within the practical range.

$$0.7\ \mu\text{m} \le L \le 2\ \mu\text{m}$$
$$400\ \mu\text{m} \le Z \le 2400\ \mu\text{m}$$
$$0.12\ \mu\text{m} \le a \le 0.5\ \mu\text{m}$$
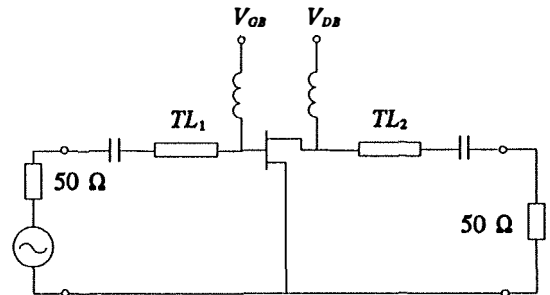$$2\times10^{22}\ \text{m}^{-3} \le N_d \le 3\times10^{23}\ \text{m}^{-3}$$

Fig. 1. The single-stage power amplifier.

In the nominal design we considered two cases using minimax optimization. In Case I the device is kept constant and the matching circuits (TL_1 and TL_2) are optimized. At the minimax solution only the specification for $P_{out}[1]$ is satisfied. The specifications for $P_{out}[2]$ and PAE are violated. In Case II we optimized both the device and the matching circuits starting at the solution of Case I. After optimization all the specifications are satisfied. The values of the design variables of both cases are listed in Table I. The power-added efficiency PAE versus input power before and after optimization of both cases is depicted in Fig. 2. From these results we can see the advantages of simultaneous device and circuit design over the conventional circuit design where only the matching circuits can be optimized.

By taking the minimax solution of Case II as the starting point we perform yield optimization using one-sided Huber optimization. A normal distribution with 3% standard deviation is assigned to the physical parameters of the MESFET, the characteristic impedance and the lengths of the transmission lines. All statistical parameters are considered independent. 100 statistical outcomes are used in yield estimation and optimization. The yield is 56% at the starting point. After optimization the yield is increased to 83%. The values of the design variables after centering are also listed in Table I. The histograms of PAE before and after design centering are plotted in Fig. 3. The run charts of $P_{out}[2]$ before and after design centering are shown in Fig. 4.

TABLE I
VALUES OF VARIABLES
FOR NOMINAL DESIGN AND DESIGN CENTERING

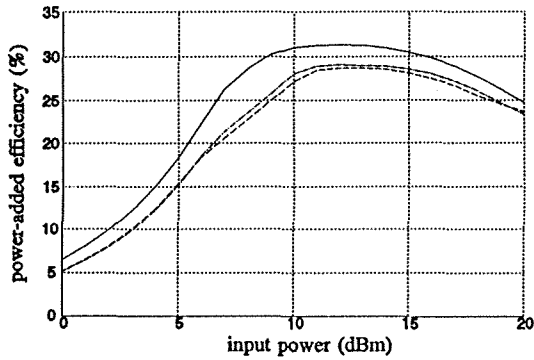| Variable | Before Optimization | Nominal Design | | Design Centering |
		Case I	Case II	
$L(\mu m)$	1.2	1.2	0.7	0.7
$a(\mu m)$	0.2	0.2	0.12	0.121
$Z(\mu m)$	1200	1200	744.85	724.68
$N_d(1/m^3)$	1.2×10^{23}	1.2×10^{23}	2.722×10^{23}	2.468×10^{23}
$TL_1(mm)$	0.5	0.649	0.118	0.116
$TL_2(mm)$	0.5	0.257	0.217	0.296

Fig. 2. The power-added efficiency versus input power before optimization (---) and after optimization of Case I (-•-) and Case II (——).
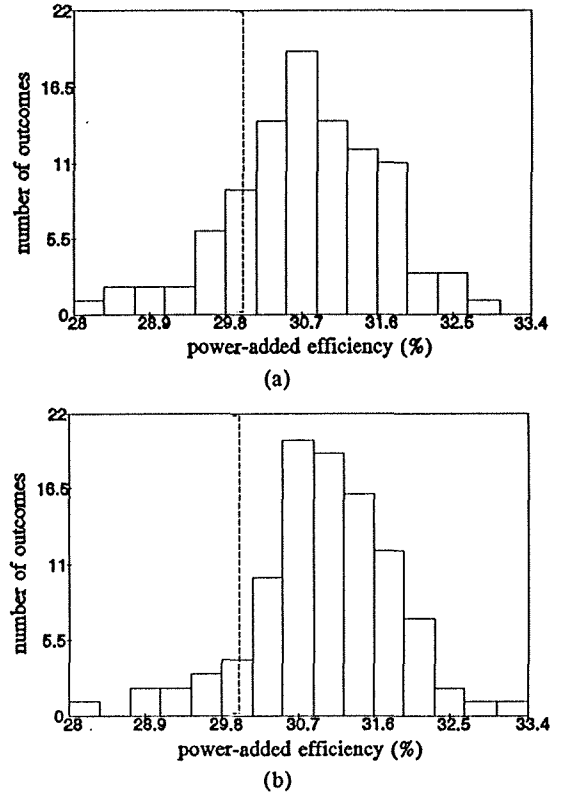

Fig. 3. Histogram of the power-added efficiency, (a) before design centering, and (b) after design centering.
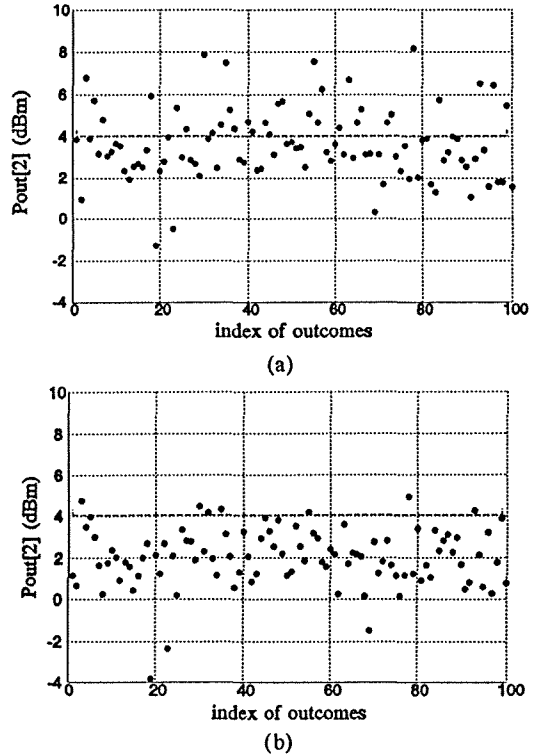

Fig. 4. Run chart of the second harmonic output power, (a) before design centering, and (b) after design centering.

3

Based on the solution of design centering we perform cost-driven design. The parameter standard deviations x_L (for FET gate length), x_Z (for FET gate width), x_a (for FET channel thickness), x_{Nd} (for FET doping density) and x_{TL} (for transmission lines TL_1 and TL_2) are selected as design variables. Five cases with specified yields of 80%, 75%, 70%, 65% and 60% are considered. The weighting factors are selected as 3, 2, 5, 2 and 1 for x_L, x_Z, x_a, x_{Nd} and x_{TL}, respectively. The values of the standard deviations before and after optimization are listed in Table II. We can observe that the standard deviations (in effect the manufacturing tolerances) could be enlarged to reduce the cost by cost-driven design subject to a specified minimum value of yield.

TABLE II
STANDARD DEVIATIONS FOR DESIGN TOLERANCING

Standard Deviation	Before Optimization	After Optimization				
		Case 1	Case 2	Case 3	Case 4	Case 5
x_L(%)	3	3.1152	3.2366	3.4590	3.7103	3.9781
x_Z(%)	3	3.0517	3.1075	3.2123	3.3351	3.4698
x_a(%)	3	3.3098	3.6150	4.1467	4.7009	5.2722
x_{Nd}(%)	3	3.0517	3.1075	3.2123	3.3351	3.4698
x_{TL}(%)	3	3.0130	3.0272	3.0545	3.0872	3.1241

Case 1: the specified yield is 80%.
Case 2: the specified yield is 75%.
Case 3: the specified yield is 70%.
Case 4: the specified yield is 65%.
Case 5: the specified yield is 60%.

CONCLUSIONS

We have addressed physics-based large-signal simultaneous device and circuit cost-driven design using the PBR model. We have presented physics-based one-sided Huber design centering. Our approach to cost-driven design by minimizing the cost function subject to a specified yield can be applied to find a compromise between yield and cost.

It should be pointed out that the physics-based models have certain limitations such as inadequate accuracy and the requirement of determining empirical fitting factors. For more accurate applications physical models (e.g., two-dimensional or quasi-two-dimensional models [14,15]) should be used. However, physical models require much more computation time than the physics-based models. Effective utilization of these two types of models will in future be achieved by our novel Space Mapping technique [6]. We believe that the Space Mapping approach will be a key technique in the next generation of microwave CAD to achieve the accuracy of physical simulation and the speed of circuit-level optimization.

REFERENCES

[1] F. Filicori, G. Ghione and C.U. Naldi, "Physics-based electron device modelling and computer-aided MMIC design," *IEEE Trans. Microwave Theory and Tech.*, vol. 40, 1992, pp. 1333-1352.

[2] D.E. Stoneking, G.L. Bilbro, P.A. Gilmore, R.J. Trew and C.T. Kelley, "Yield optimization using a GaAs process simulator coupled to a physical device model," *IEEE Trans. Microwave Theory and Tech.*, vol. 40, 1992, pp. 1353-1363.

[3] E.M. Bastida, G.P. Donzelli and M. Pagani, "Efficient development of mass producible MMIC circuits," *IEEE Trans. Microwave Theory and Tech.*, vol. 40, 1992, pp. 1364-1373.

[4] J.W. Bandler, R.M. Biernacki, Q. Cai, S.H. Chen, S. Ye and Q.J. Zhang, "Integrated physics-oriented statistical modeling, simulation and optimization," *IEEE Trans. Microwave Theory Tech.*, vol. 40, 1992, pp. 1374-1400.

(5) C.M. Snowden, "Nonlinear modelling of power FETs and HBTs," *Third Int. Workshop on Integrated Nonlinear Microwave and Millimeterwave Circuits INMMC'94 Dig.* (Duisburg, Germany), 1994, pp. 11-25.

(6) J.W. Bandler, R.M. Biernacki, S.H. Chen, P.A. Grobelny, C. Moskowitz and S.H. Talisa, "Electromagnetic design of high-temperature superconducting microwave filters," *IEEE MTT-S Int. Microwave Symp. Dig.* (San Diego, CA), 1994, pp. 993-996.

[7] A. Madjar and F.J. Rosenbaum, "A large-signal model for the GaAs MESFET," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, 1981, pp. 781-788.

[8] M.A. Khatibzadeh and R.J. Trew, "A large-signal, analytic model for the GaAs MESFET," *IEEE Trans. Microwave Theory Tech.*, vol. 36, 1988, pp. 231-238.

[9] S. D'Agostino, G. D'Inzeo, P. Marietti, L. Tudini and A. Betti-Berutto, "Analytic physics-based expressions for the empirical parameters of the Statz-Pucel MESFET model," *IEEE Trans. Microwave Theory Tech.*, vol. 40, 1992, pp. 1576-1581.

[10] H. Statz, P. Newman, I.W. Smith, R.A. Pucel and H.A. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. Electron Devices*, vol. ED-34, 1987, pp. 160-169.

[11] *OSA90/hope™* and *OSA90/hope™ Applications Illustrated*, Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7, 1994.

[12] J.W. Bandler, S.H. Chen, R.M. Biernacki and K. Madsen, "The Huber concept in device modeling, circuit diagnosis and design centering," *Proc. IEEE Int. Symp. Circuits and Systems* (London, England), 1994, vol. 1, pp. 129-132.

[13] J.W. Bandler and S.H. Chen, "Circuit optimization: the state of the art," *IEEE Trans. Microwave Theory Tech.*, vol. 36, 1988, pp. 424-443.

[14] C.M. Snowden and D. Loret, "Two-dimensional hot electron models for short gate length GaAs MESFETs" *IEEE Trans. Electron Devices*, vol. ED-34, 1987, pp. 212-223.

[15] C.M. Snowden and R.R. Pantoja, "Quasi-two-dimensional MESFET simulations for CAD" *IEEE Trans. Electron Devices*, vol. ED-36, 1989, pp. 1564-1574.