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SIMULTANEOUS DEVICE AND CIRCUIT DESIGN**

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**SOS-94-9-R**

**October 1994**

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SIMULTANEOUS DEVICE AND CIRCUIT DESIGN**

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*Abstract*

We present a cost-driven approach to the emerging demand for simultaneous device and circuit design. Here, an analytic physics-based Raytheon model facilitates fast large-signal simulation and optimization. A novel one-sided Huber approach is applied to design centering. The problem of cost-driven design is formulated as the minimization of the cost function while maintaining the required yield. Devices and matching circuits are optimized simultaneously, the advantages of which are demonstrated by a single-stage power amplifier design.

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This work was supported in part by the Natural Sciences and Engineering Research Council of Canada under Grant STR0117819 and in part by Optimization Systems Associates Inc. . Additional support was provided through a Natural Sciences and Engineering Research Council of Canada Industrial Research Fellowship granted to Q. Cai.

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## SUMMARY

### *Introduction*

Automated physics-based CAD directly links the physical parameters (geometrical, material, process) with performance and yield specifications in MMIC design. The potential advantages of optimization-driven physics-based CAD have been demonstrated in a number of publications, e.g., [1-4]. The advent of more powerful computers has increased the drive in using physical models and physics-based models for microwave CAD to meet the requirement of predictability and economization [5]. Space Mapping [6] will pave the way to automating the link between physics-based and physical simulations.

Statistical design centering (yield optimization) has been considered as indispensable for the design of MMICs where all the active and passive components are fabricated on a common semi-insulating substrate (e.g. [1-5]). Post-production tuning of MMICs is restricted, and device replacement is not possible. The production yield depends on parameters such as nominal values, tolerances and uncertainties. Yield optimization maximizes the yield by optimizing the nominal values of the design variables while keeping tolerances constant. However, the cost for obtaining such tolerances may be high. There is a trade-off between the yield and the cost. Therefore, cost-driven design is necessary for minimizing the cost while maintaining the required yield.

Device modeling is the basis for circuit simulation and optimization. A number of large-signal analytical physics-based GaAs MESFET models have been developed during the last decade, e.g., [7, 8]. Those models involve iterations to solve for an intermediate parameter  $v_1$  which requires certain computational effort. Therefore, they are not efficient enough for cost-driven design when a large number of circuits have to be repeatedly simulated. To facilitate fast large-signal simulation and optimization we use the physics-based Raytheon (PBR) model [9] where the empirical parameters of the Raytheon model [10] are calculated from the physical parameters using analytical formulas. The PBR is implemented in conjunction with the built-in Raytheon model (FETR) of OSA90/hope [11].

We present, for the first time, a one-sided Huber approach [12] to physics-based design

centering. The design centering problem is formulated using the one-sided Huber function to maximize design yield. The problem of cost-driven design is formulated as the minimization of the cost function [13, 14] subject to a specified yield.

The advantages of our approach are demonstrated by a single-stage power amplifier design. The physical parameters of the device, such as FET gate length, channel thickness and doping density, and the elements of the matching circuits are optimized simultaneously.

Our approach is implemented in the CAD system OSA90/hope which is used to generate all the results presented in this paper.

### Physics-Based Raytheon Model

In the Raytheon model [9] the drain current  $I_d$  of a FET is calculated by

$$I_d = \begin{cases} \frac{\beta[v_{gs}(t - \tau) - V_{T0}]^2}{1 + \theta[v_{gs}(t - \tau) - V_{T0}]} \left[ 1 - \left( 1 - \frac{\alpha v_{ds}}{3} \right)^3 \right] (1 + \lambda v_{ds}) & \text{for } 0 < v_{ds} < \frac{3}{\alpha} \\ \frac{\beta[v_{gs}(t - \tau) - V_{T0}]^2}{1 - \theta[v_{gs}(t - \tau) - v_{T0}]} (1 + \lambda v_{ds}) & \text{for } v_{ds} \geq \frac{3}{\alpha} \end{cases} \quad (1)$$

where  $\alpha$ ,  $\beta$ ,  $\lambda$ ,  $\theta$ ,  $\tau$  and  $V_{T0}$  are empirical model parameters. To obtain the PBR model we calculate the empirical model parameters using the analytical expressions derived by D'Agostino *et al.* [9].

For example,

$$\alpha = \frac{V_{p0} + 3E_s \left[ L - \frac{2a}{\pi} \sinh^{-1} \left( \frac{\pi K_d}{2aE_s} \right) \right]}{E_s L \left( 1 - \sqrt{\frac{E_s L}{V_{p0} + E_s L}} \right) (V_{p0} + 3E_s L)} \quad (2)$$

$$\beta = \frac{q \mu_0 N_d Z a \xi (V_{p0} + 3E_s L) \left( 1 - \sqrt{\frac{\xi}{1 - \xi}} \right) (2 + \xi^2)}{L V_{p0} [V_{p0} + 3E_s (L - L_s)] (1 + \xi^2)} \quad (3)$$

where

$$L_s = \frac{2a}{\pi} \sinh^{-1} \left[ \frac{\pi K_d}{2aE_s} \left( \frac{3}{\alpha} - \frac{E_s L V_{p0}}{E_s L + V_{p0}} \right) \right] \quad (4)$$

$$\xi = \frac{E_s L}{V_{p0}} \quad (5)$$

$$V_{p0} = \frac{q N_d a^2}{2\epsilon} \quad (6)$$

$$V_{T0} = V_{bi} - V_{p0} \quad (7)$$

are the length of velocity saturation region under the gate, the saturation index, the ideal pinch-off voltage and the threshold voltage, respectively. The physical parameters of the PBR model include  $L$  the gate length,  $a$  the channel thickness,  $Z$  the gate width,  $E_s$  the electric field value at the electron drift velocity saturation,  $q$  the electron charge,  $\mu_0$  the low-field electron mobility,  $N_d$  the doping density,  $\epsilon$  the dielectric permittivity and  $V_{bi}$  the built-in voltage.  $K_d$  is the domain parameter [9].

Since analytical expressions are used in the computations of the PBR model it is very efficient for large-signal circuit simulation and optimization, particularly for cost-driven design. The accuracy of the PBR has been demonstrated in [9] by comparing the DC characteristics of the model with those of the measured data.

### *Design Centering Using the One-Sided Huber Function*

In statistical design centering a number of statistical outcomes of circuit parameters, denoted by  $\phi^i$ , are considered. In our physics-based design centering  $\phi^i$  include the physical parameters of the devices and the parameters of the matching circuit elements. The design yield can be estimated as

$$Y = \frac{N_a}{N} \quad (8)$$

where  $N_a$  is the number of acceptable outcomes and  $N$  is the total number of outcomes considered.

Following the method of Bandler and Chen [13], for each outcome we create a generalized  $\ell_p$  function  $\nu(\phi^i)$  whose value is zero or negative if the outcome is acceptable. The design centering

problem is then formulated as the minimization of the objective function  $U(\phi^0)$  defined by [12]

$$U(\phi^0) = \sum_{i=1}^N \rho_k^+[\alpha_i \nu(\phi^i)] \quad (9)$$

where  $\phi^0$  is the nominal circuit parameters to be centered,  $\alpha_i$  is a positive multiplier associated with the  $i$ th outcome,  $\rho_k^+$  is the one-sided Huber function defined by

$$\rho_k^+(f) = \begin{cases} 0 & \text{if } f \leq 0 \\ f^2/2 & \text{if } 0 < f \leq k \\ kf - k^2/2 & \text{if } f > k \end{cases} \quad (10)$$

and  $k$  is a positive constant threshold value ( $f$  is an error function which is  $\alpha_i \nu(\phi^i)$  in our case).

#### *Formulation of Cost-Driven Design*

In Monte Carlo simulation a statistical outcome  $\phi^i$  can be represented by

$$\phi^i = \phi^0 + \Delta\phi^i \quad (11)$$

where the random perturbation  $\Delta\phi^i$  depends on the tolerances (standard deviations in normal distributions) of the parameter statistical distributions. Let

$$\mathbf{x} = [x_1 \ x_2 \ \dots \ x_m]^T \quad (12)$$

be the parameter tolerance vector where  $m$  is the total number of statistical variables. In the yield optimization problem  $\mathbf{x}$  is kept constant while optimizing the parameter nominal value  $\phi^0$  to increase the yield. In the present implementation of cost-driven design  $\phi^0$  is kept constant and  $\mathbf{x}$  is optimized to reduce the cost since the larger the parameter tolerances the lower the cost. We formulate the problem of cost-driven design as

$$\begin{aligned} & \underset{\mathbf{x}}{\text{minimize}} \quad C(\mathbf{x}) \\ & \text{subject to} \quad Y \geq Y_S \end{aligned} \quad (13)$$

where  $Y$  is the design yield defined in (8),  $Y_S$  is the specified yield and  $C(\mathbf{x})$  is the cost function.

In our calculation we use the cost function defined by [13, 14]

$$C(\mathbf{x}) = \sum_{i=1}^m \frac{c_i}{x_i} \quad (14)$$

where  $c_i$  is a nonnegative weighting factor associated with the  $i$ th design variable.

### *A Single-Stage Power Amplifier Design*

As an example we consider a single-stage power amplifier shown in Fig. 1. The design is based on the circuit structure described in [15]. The amplifier is designed as Class-A. The design specifications are at 10 GHz frequency and 10 dBm input power

$$\begin{aligned} P_{out}[1] &\geq 26 \text{ dBm} \\ P_{out}[2] &\leq 4 \text{ dBm} \\ PAE &\geq 30 \% \end{aligned}$$

where  $P_{out}[1]$  and  $P_{out}[2]$  are the fundamental output power and the second harmonic output power, respectively,  $PAE$  is the power-added efficiency. We performed nominal design, yield optimization and cost-driven design using OSA90/hope. The gate length  $L$ , gate width  $Z$ , channel thickness  $a$  and the doping density  $N_d$  of the MESFET, the physical lengths of transmission lines  $TL_1$  and  $TL_2$  in the matching circuits are chosen as design variables. The following constraints are imposed on the design variables of the MESFET in order to guarantee that their values are within the practical range.

$$\begin{aligned} 0.7 \mu\text{m} &\leq L \leq 2 \mu\text{m} \\ 400 \mu\text{m} &\leq Z \leq 2400 \mu\text{m} \\ 0.12 \mu\text{m} &\leq a \leq 0.5 \mu\text{m} \\ 2 \times 10^{22} \text{ m}^{-3} &\leq N_d \leq 3 \times 10^{23} \text{ m}^{-3} \end{aligned}$$

In the nominal design we considered two cases using minimax optimization. In Case I the device is kept constant and the matching circuits ( $TL_1$  and  $TL_2$ ) are optimized. At the minimax solution only the specification for  $P_{out}[1]$  is satisfied. The specifications for  $P_{out}[2]$  and  $PAE$  are violated. In Case II we optimized both the device and the matching circuits starting at the solution of Case I. After optimization all the specifications are satisfied. The values of the design variables of both cases are listed in Table I. The second harmonic output power  $P_{out}[2]$  and the power-added efficiency  $PAE$  versus input power before and after optimization of both cases are depicted in Fig.

2. From these results we can see the advantages of simultaneous device and circuit design over the conventional circuit design where only the matching circuits can be optimized.

By taking the minimax solution of Case II as the starting point we perform yield optimization using one-sided Huber optimization. A normal distribution with 3% standard deviation is assigned to the physical parameters of the MESFET, the characteristic impedance and the lengths of the transmission lines. All statistical parameters are considered independent. 100 statistical outcomes are used in yield estimation and optimization. The yield is 56% at the starting point. After optimization the yield is increased to 83%. The values of the design variables before and after centering are listed in Table II. The histograms of  $P_{out}[2]$  and  $PAE$  before and after design centering are plotted in Figs. 3 and 4, respectively. The run chart of  $P_{out}[2]$  and  $PAE$  before and after design centering are shown in Figs. 5 and 6, respectively.

Based on the solution of design centering we perform cost-driven design. The parameter standard deviations  $x_L$  (for FET gate length),  $x_Z$  (for FET gate width),  $x_a$  (for FET channel thickness),  $x_{Nd}$  (for FET doping density) and  $x_{TL}$  (for transmission lines  $TL_1$  and  $TL_2$ ) are selected as design variables. Five cases with specified yields of 80%, 75%, 70%, 65% and 60% are considered. The weighting factors are selected as 3, 2, 5, 2 and 1 for  $x_L$ ,  $x_Z$ ,  $x_a$ ,  $x_{Nd}$  and  $x_{TL}$ , respectively. The values of the standard deviations before and after optimization are listed in Table III. We can observe that the standard deviations (in effect the manufacturing tolerances) could be enlarged to reduce the cost by cost-driven design subject to a specified minimum value of yield.

### *Conclusions*

We have addressed physics-based large-signal simultaneous device and circuit cost-driven design using the PBR model. We have presented physics-based one-sided Huber design centering. Our approach to cost-driven design by minimizing the cost function subject to a specified yield can be applied to find a compromise between yield and cost.

It should be pointed out that the physics-based models have certain limitations such as inadequate accuracy and the requirement of determining empirical fitting factors. For more

accurate applications physical models (e.g., two-dimensional or quasi-two-dimensional models [16, 17]) should be used. However, physical models require much more computation time than the physics-based models. Effective utilization of these two types of models will in future be achieved by our novel Space Mapping [6], which will be our next research focus. We believe that the Space Mapping technique will be a key technique in the next generation of microwave CAD to achieve the accuracy of physical simulation and the speed of circuit-level optimization.

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TABLE I

VALUES OF VARIABLES FOR NOMINAL DESIGN

Variable	Before Optimization	After Optimization	
		Case I	Case II
$L(\mu\text{m})$	1.2	1.2	0.7
$a(\mu\text{m})$	0.2	0.2	0.12
$Z(\mu\text{m})$	1200	1200	744.85
$N_d(1/\text{m}^3)$	$1.2 \times 10^{23}$	$1.2 \times 10^{23}$	$2.722 \times 10^{23}$
$TL_1(\text{mm})$	0.5	0.649	0.118
$TL_2(\text{mm})$	0.5	0.257	0.217

TABLE II

VALUES OF VARIABLES FOR DESIGN CENTERING

Variable	Before Optimization	After Optimization
$L(\mu\text{m})$	0.7	0.7
$a(\mu\text{m})$	0.12	0.121
$Z(\mu\text{m})$	744.85	724.68
$N_d(1/\text{m}^3)$	$2.722 \times 10^{23}$	$2.468 \times 10^{23}$
$TL_1(\text{mm})$	0.118	0.116
$TL_2(\text{mm})$	0.217	0.296

TABLE III

STANDARD DEVIATIONS FOR DESIGN TOLERANCING

Standard Deviation	Before Optimization	After Optimization				
		Case 1	Case 2	Case 3	Case 4	Case 5
$x_L(\%)$	3	3.1152	3.2366	3.4590	3.7103	3.9781
$x_Z(\%)$	3	3.0517	3.1075	3.2123	3.3351	3.4698
$x_a(\%)$	3	3.3098	3.6150	4.1467	4.7009	5.2722
$x_{Nd}(\%)$	3	3.0517	3.1075	3.2123	3.3351	3.4698
$x_{TL}(\%)$	3	3.0130	3.0272	3.0545	3.0872	3.1241

Case 1: the specified yield is 80%.  
 Case 2: the specified yield is 75%.  
 Case 3: the specified yield is 70%.  
 Case 4: the specified yield is 65%.  
 Case 5: the specified yield is 60%.

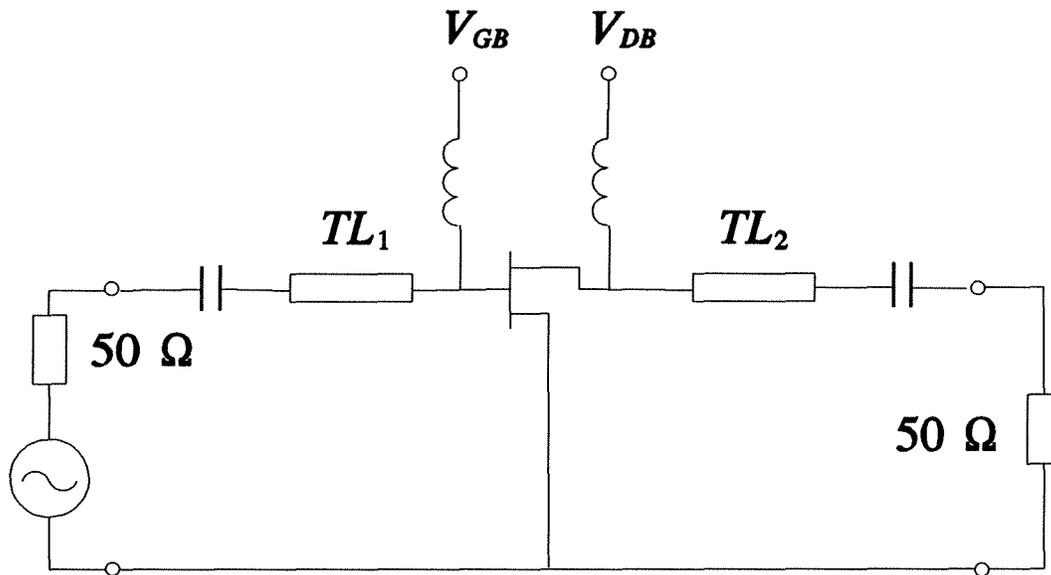
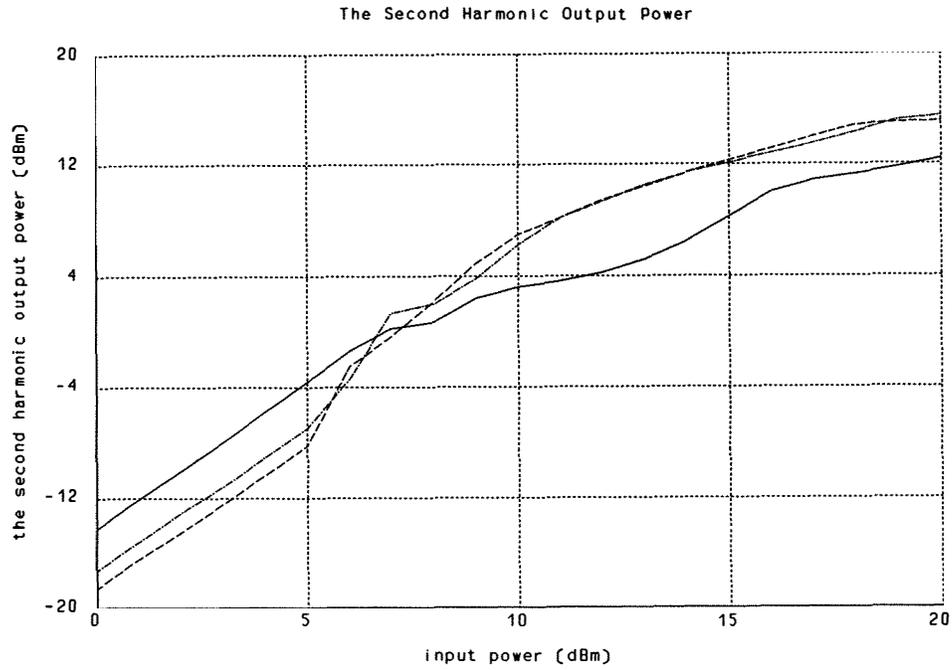
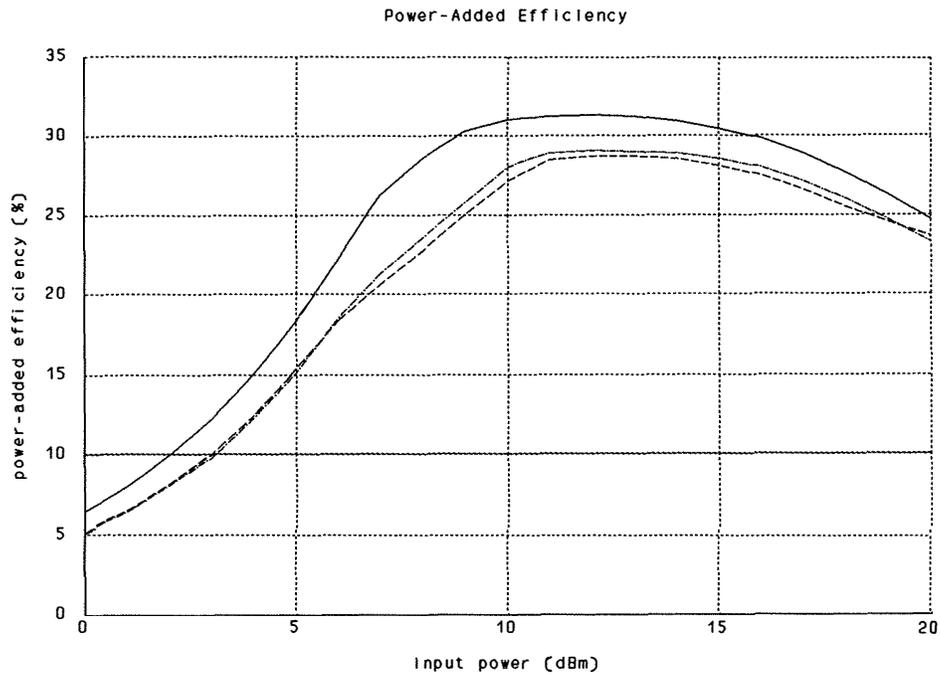


Fig. 1. The single-stage power amplifier.

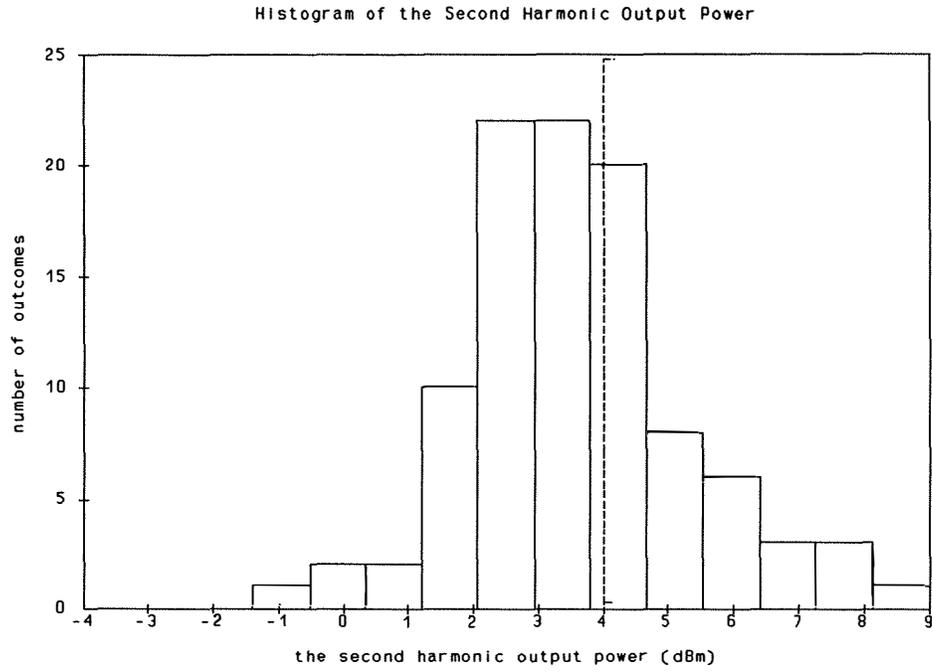


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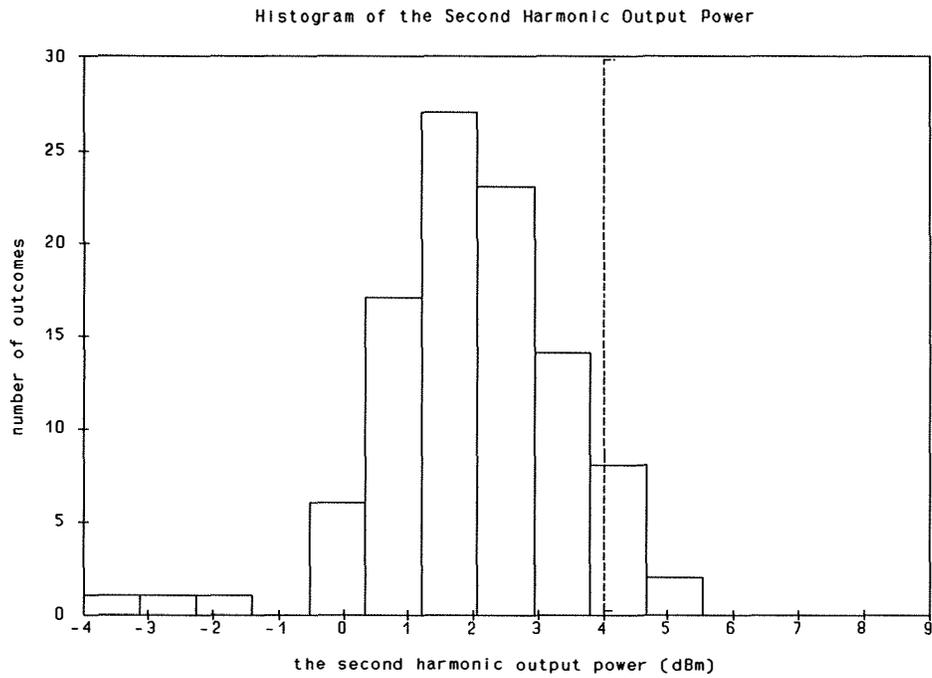


(b)

Fig. 2. (a) The second harmonic output power, (b) the power-added efficiency versus input power before optimization (---) and after optimization of Case I (-.-) and Case II (—).

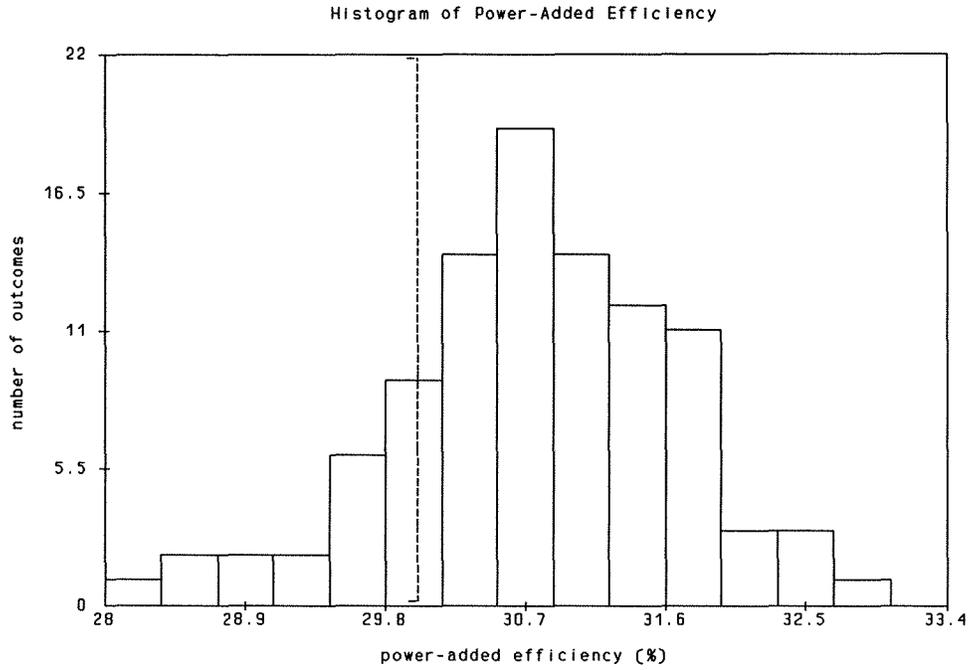


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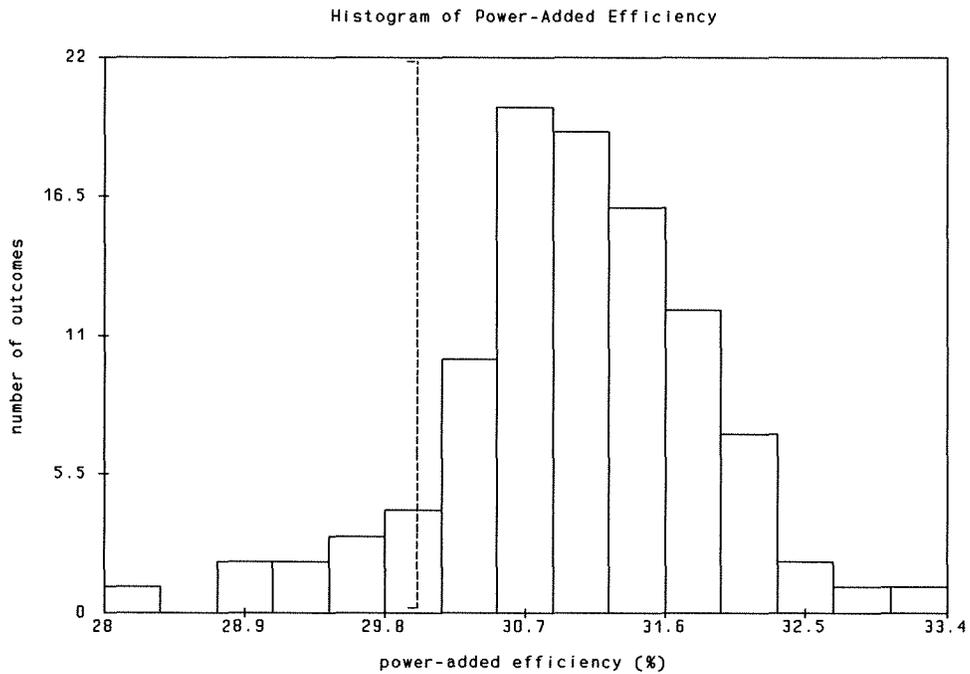


(b)

Fig. 3. Histogram of the second harmonic output power, (a) before design centering, and (b) after design centering.

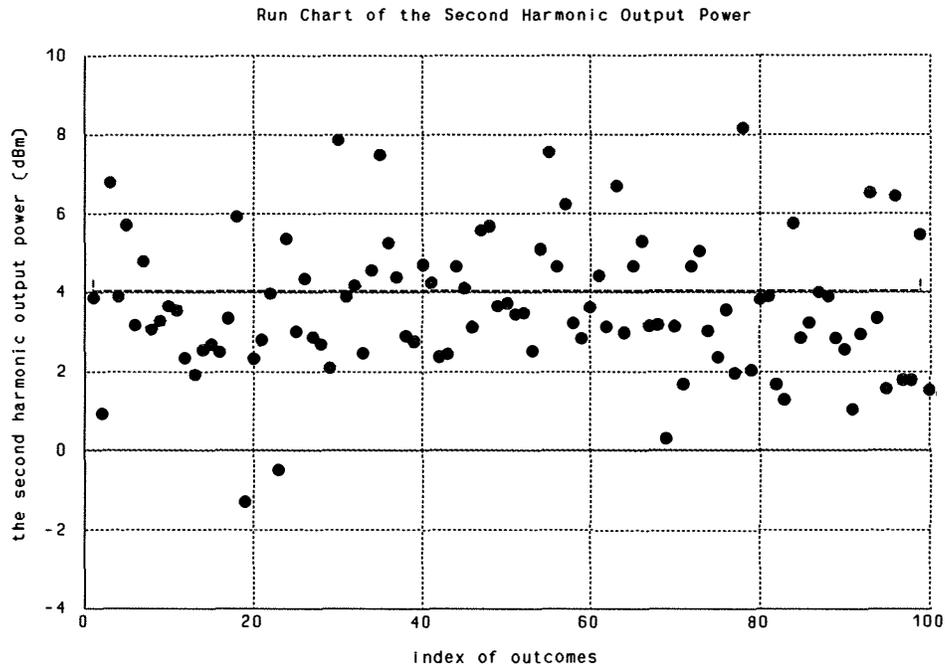


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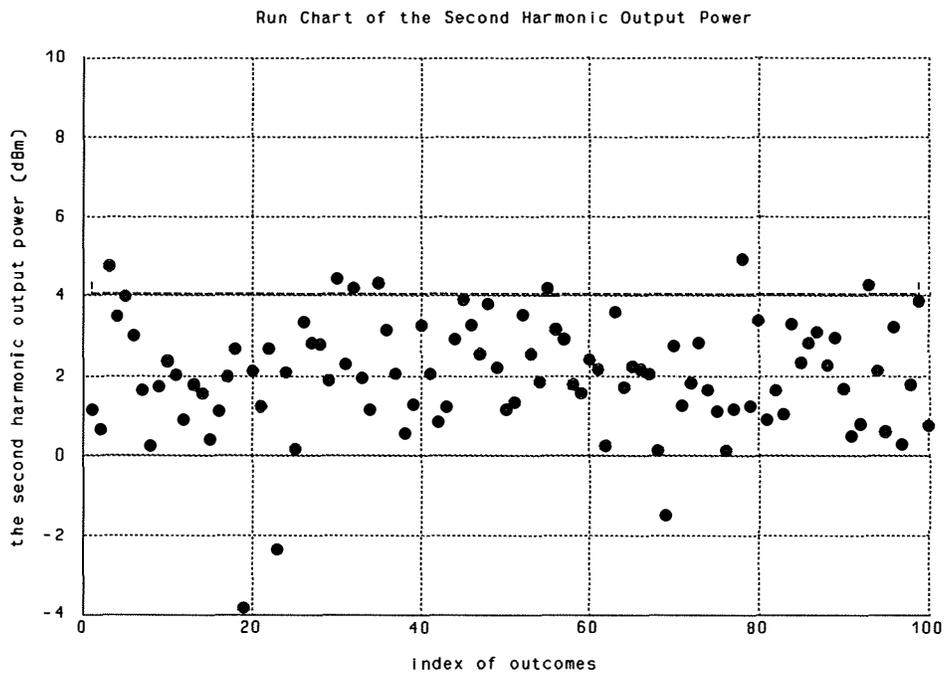


(b)

Fig. 4. Histogram of the power-added efficiency, (a) before design centering, and (b) after design centering.

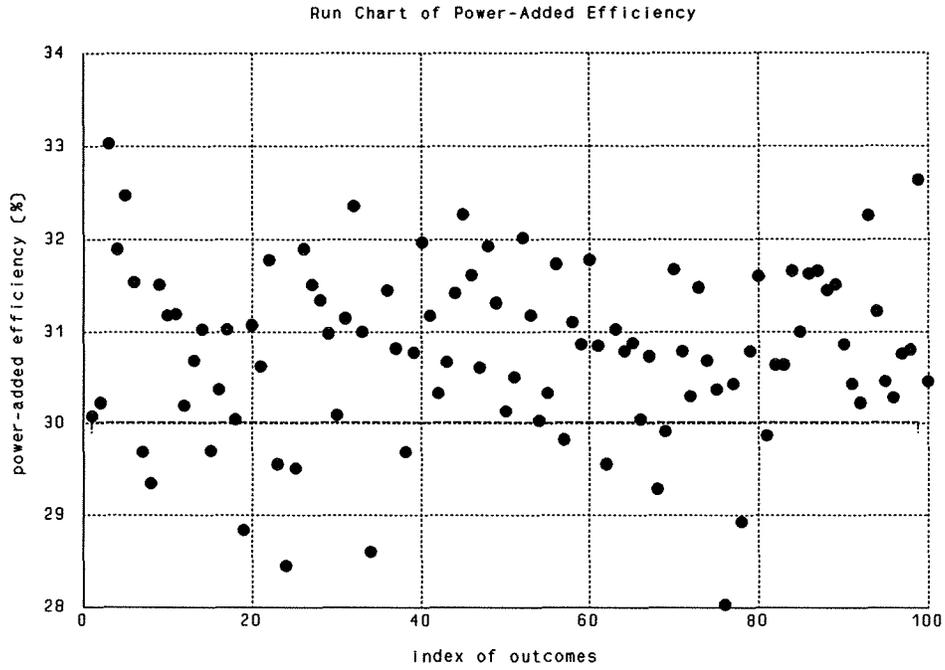


(a)

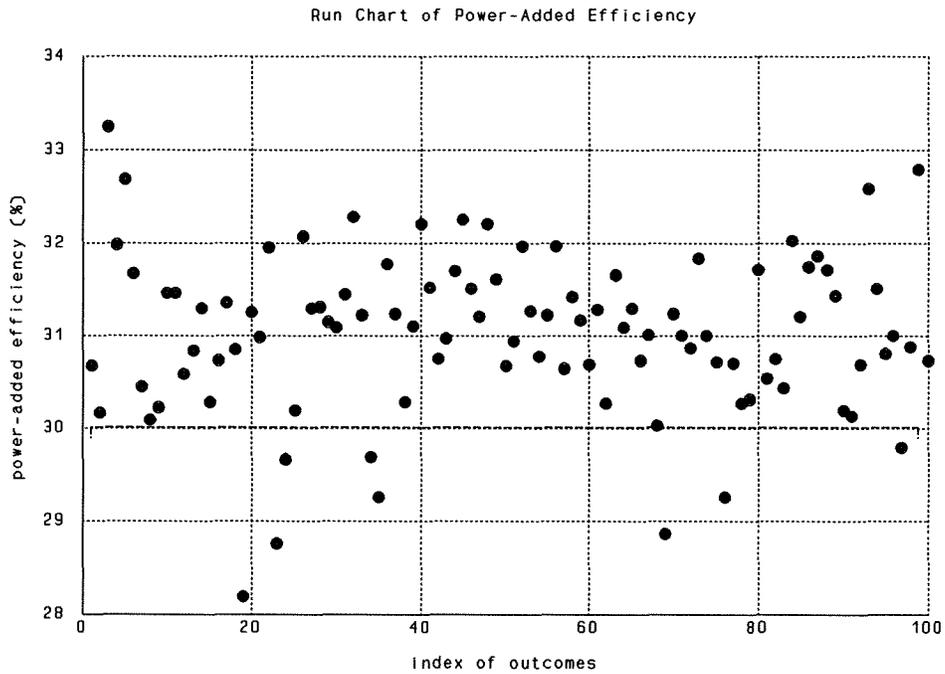


(b)

Fig. 5. Run chart of the second harmonic output power, (a) before design centering, and (b) after design centering.



(a)



(b)

Fig. 6. Run chart of the power-added efficiency, (a) before design centering, and (b) after design centering.