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YIELD OPTIMIZATION FOR ARBITRARY STATISTICAL DISTRIBUTIONS

PART II: IMPLEMENTATION

H.L. Abdel-Malek and J.W. Bandler

Group on Simulation, Optimization and Control
and Department of Electrical Engineering
McMaster University, Hamilton, Canada

ABSTRACT

A suggested test problem for proposed algorithms in yield optimization is described in detail. The problem is a current switch emitter follower (CSEF) circuit originally described by Ho, which includes a transmission line. The ideas presented in Part I of this paper are applied to this circuit in order to obtain an optimal statistical design using realistic correlations between transistor model parameters.

INTRODUCTION

Need is growing for test problems in the area of yield optimization. Yield optimization has been considered by Elias [1] and by Becker and Jensen [2] using the Monte Carlo method of yield analysis. It was also considered by Bandler and Abdel-Malek [3] using linear cuts but for uniform distribution of outcomes.

A current switch emitter follower circuit which was previously investigated by Ho [4] in the context of sensitivity calculations is chosen for implementing the ideas presented in Part I of this paper. A detailed description of the circuit is given. Felt to be a worthwhile preliminary exercise to statistical design, an optimal worst-case design is carried out. Sparsity is exploited in developing the quadratic models for the constraints.

Correlations between transistor model parameters through formulas based on work published by Balaban and Golembeski [5] are established. According to these correlations, weights to be assigned to the orthocells are computed (see Part I of this paper). Production yield is maximized employing analytical formulas for yield and its sensitivities as well as the quadratic approximations to the design constraints. It is shown how different design specifications can be investigated and corresponding optimal yields obtained without any additional circuit simulations.

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ANALYSIS OF THE CSEF

The circuit is shown in Fig. 1. The decoupled equivalent circuit of the transmission line is used. Considering a lossless transmission line and the charge-control model of the transistors as well as the diode the circuit is shown in Fig. 2. The following two equations are used for the transmission line model.

$$u_i(t) = [e_0(t-\tau) + Z_0\, i_0(t-\tau)]\, U(t-\tau) + \Phi_i(t),$$
$$u_r(t) = [e_\ell(t-\tau) + Z_0\, i_\ell(t-\tau)]\, U(t-\tau) + \Phi_r(t),$$

where Z_0 and τ are the characteristic impedance and the delay time of the transmission line, respectively, U is the step function given by

$$U(t-\tau) = \begin{cases} 0 & t < \tau, \\ 1 & t \geq \tau. \end{cases}$$

The parameter Φ represents the initial voltage distribution stored on the transmission line. Thus, we take

$$\Phi_i(t) = \Phi_r(t) = 0 \quad \text{for } t \geq \tau.$$

The original circuit parameters and model parameters are given in Table I.

The Subroutine DVOGER [6], based on Gear's integration algorithm [7], was used.

WORST-CASE DESIGN OF THE CSEF

The parameter vector considered for a worst-case design (see Fig. 2) is

$$(\underset{\sim}{\phi})^T = [E_4\ Z_0\ R_4\ C_0].$$

The corresponding tolerances are denoted by ϵ_1, ϵ_2, ϵ_3 and ϵ_4. Fig. 3 shows the input voltage E_1 and the time point constraints used. The response obtained with the parameter values in Table I are also shown. The circuit is initially at equilibrium with $E_1 = -0.776$ V. The values of the constraints g_i are obtained from the circuit response and the specifications shown in Fig. 3. Each constraint g_i is described by a quadratic polynomial P_i having 15 coefficients.

The nonlinear program formulated to solve the

worst-case design problem [3] is

$$\underset{\underset{\sim}{\phi}^0,\ \underset{\sim}{\varepsilon}}{\text{minimize}}\ E_4^0/\varepsilon_1 + Z_0^0/\varepsilon_2 + R_4^0/\varepsilon_3 + C_0^0/\varepsilon_4$$

subject to

$$P_i(\underset{\sim}{\phi}^r) \geq 0,\ r = 1, 2, \ldots, 2^4,$$

$$i = 1, 2, \ldots, 7,$$

where $\underset{\sim}{\phi}^r$ indicates a vertex of the tolerance orthotope as given by equation (6) of Part I. The output capacitor C_0 was constrained such that

$$C_0^0 - \varepsilon_4 \geq 1.0 \text{ pF}.$$

This constraint was designed to prevent an unrealistic nominal value.

Starting at the nominal parameter values given in Table I and according to the algorithm published in [3], the approximations were updated once. The program FLOPT4 [8] was used for solving this nonlinear programming problem. The optimal worst-case nominal parameters and tolerances are shown in Table II. The nominal design response as well as the responses for the critical vertices, numbered according to equation (7) of Part I, are shown in Fig. 3.

A single interpolation region was found to be satisfactory. The difference between the predicted responses at vertices according to the approximations and the actual responses subsequently checked by integration was, over the sample points used, less than 2%.

For the worst-case design obtained the power dissipated in the output circuit is 0.1854 mW at the nominal solution. It is 0.365 mW for the original design at equilibrium when $E_1 = -0.776$. This saves power and limits fluctuations in chip temperature.

STATISTICAL DESIGN OF THE CSEF

The output section of the CSEF circuit was optimally designed to provide maximum yield. The statistical distributions of the circuit parameters and the transistor model parameters were assumed to be fixed. The nominal values of the output circuit parameters were optimized in order to obtain maximum yield.

The statistical distributions of the transistor T_3 model parameters are based upon results published by Butler [9] and by Balaban and Golembeski [5]. The transistor current gain β was assumed to have a triangular probability distribution function with a peak at $\beta = 60$ and $40 \leq \beta \leq 100$. Correlation between transistor model parameters (see Table I(c)) was established according to the following equations

$$I_S = 0.0061\ \beta\ (1 + 0.3516\ X_{r1}) \times 10^{-9}\ \text{A},$$

$$C_{JE} = (0.144 - 0.242 \times 10^{-3}\beta)\ (1 + 0.2\ X_{r2})\ \text{pF},$$

$$TT = 0.01\ (1 + 0.2\ X_{r3})\ \text{ns},$$

where X_{ri} are independent uniformly distributed random numbers over the range

$$-1 \leq X_{ri} \leq 1,\ i = 1, 2, 3.$$

According to these distributions the weights and intervals for the discretized distribution were determined and are shown in Table III.

The circuit parameters were assumed to have the distributions

$$E_4 = E_4^0 + 0.1632\ X_{r4}, \quad Z_0 = Z_0^0 + 9.5\ X_{r5},$$

$$R_4 = R_4^0 + 4.4\ X_{r6}, \quad C_0 = C_0^0 + 0.27\ X_{r7},$$

where, again,

$$-1 \leq X_{ri} \leq 1,\ i = 4, 5, 6, 7.$$

The nonlinear programming problem to be solved is

$$\underset{\underset{\sim}{\phi}^0}{\text{maximize}}\ Y$$

subject to

$$C_0^0 \geq 1.27 \text{ pF}, \qquad Z_0^0 \leq Z_{0u},$$

where Z_{0u} is an upper bound on the characteristic impedance of the transmission line and

$$(\underset{\sim}{\phi}^0)^T = [E_4^0\ Z_0^0\ R_4^0\ C_0^0].$$

The production yield Y is calculated using equations (50) and (42) of Part I. The linear cuts are obtained from the quadratic approximations to the design constraints

$$V_0(t) \leq -1.45 \text{ V}, \quad t = 0.3 \text{ ns},$$
$$V_0(t) \geq -0.85 \text{ V}, \quad t = 0.62, 0.69, 0.8 \text{ ns},$$
$$V_0(t) \leq -1.40 \text{ V}, \quad t = 1{,}02, 1.09, 1.2 \text{ ns},$$

using equation (32) of Part I, where

$$(\underset{\sim}{\phi}^a)^T = [(\underset{\sim}{\phi}^0)^T\ \alpha_3\ I_{S3}\ C_{JE3}\ TT_3].$$

The value of $\underset{\sim}{\phi}^0$ is varying as determined during the optimization process while the remaining parameters have the fixed values given in Table IV.

A single quadratic approximation to the design constraints was carried out at the interpolation region defined by the center and size shown in Table IV. The number of response evaluations required in order to obtain these approximations is 45. This is the same as the number of coefficients of the quadratic polynomial, see equation (10) of Part I, for this 8-dimensional problem.

The weight assigned for each orthocell is obtained by multiplying the corresponding weight resulting from the correlations between the

transistor model parameters, given in Table III, by the weights for the remaining uniformly distributed independent parameters. For a uniformly distributed parameter we have $w_i(0) = w_i(2) = 0.0$, $w_i(1) = 1.0$. The yield sensitivities required during optimization are evaluated using equation (58) of Part I.

The results obtained for two different upper bounds on the characteristic impedance Z_0 are shown in Table V. These results may be compared with those obtained from 1000 Monte Carlo points, generated according to the assumed statistical distribution in conjunction with the quadratic approximations. The resulting yields are also tabulated in Table V.

In order to further demonstrate the benefits of having an approximation, the specified switching levels were varied as tabulated in Table VI and hence the corresponding constraints are simply generated by changing the constant term in the quadratic approximations. The resulting optimum yields and corresponding nominal values for the circuit parameters are given in Table VI.

The design constraints at t = 1.02 ns and at t = 1.09 ns were found to be overlapping. This is simply discovered by checking the reference vertices and the corresponding distances from them to the points of intersection of the linear cuts with the orthotope edges which are given by equations (33) and (35) of Part I, respectively. The constraint at t = 1.02 ns was removed from the optimization process since it has the same reference vertex as the constraint at t = 1.09 and its contribution to the weighted nonfeasible hypervolume is negligible.

CONCLUSIONS

Yield optimization of the CSEF circuit has been successfully performed. It has been demonstrated how small a number of simulations is required: 75 integrations for the whole investigation. This number of simulations is much smaller than the number of Monte Carlo analyses, used in such a case, to provide even a single yield estimate let alone a complete optimization. Having approximations to the design constraints allowed us to consider different design specifications without any additional circuit simulations. Furthermore, different statistical distributions can be investigated. Similar transistors manufactured under different physical conditions, for example, can be readily investigated for optimum yield without additional integrations. A full description of this work including the formulation of the state equations is available [10].

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REFERENCES

[1] N.J. Elias, "New statistical methods for assigning device tolerances", Proc. 1975 IEEE Symp. on Circuits and Systems (Newton, MA, April 1975), pp. 329-332.

[2] P.W. Becker and F. Jensen, Design of Systems and Circuits for Maximum Reliability or Maximum Production Yield. Lyngby, Denmark: Polyteknisk Forlag, 1974.

[3] J.W. Bandler and H.L. Abdel-Malek, "Optimal centering, tolerancing and yield determination using multidimensional approximations", Proc. 1977 IEEE Symp. on Circuits and Systems (Phoenix, AZ, April 1977), pp. 219-222.

[4] C.W. Ho, "Time-domain sensitivity computation for networks containing transmission lines", IEEE Trans. Circuit Theory, vol. CT-18, Jan. 1971, pp. 114-122.

[5] P. Balaban and J.J. Golembeski, "Statistical analysis for practical circuit design", IEEE Trans. Circuits and Systems, vol. CAS-22, Feb. 1975, pp. 100-108.

[6] Subroutine DVOGER, International Mathematical and Statistical Libraries, IMSL Library 3, Edition 5, (FORTRAN) CDC 6000/7000, 1975.

[7] C.W. Gear, "The automatic integration of differential equations", Comm. ACM, vol. 14, March 1971, pp. 176-179.

[8] J.W. Bandler and D. Sinha, "FLOPT4 - a program for least pth optimization with extrapolation to minimax solutions", Faculty of Engineering, McMaster University, Hamilton, Canada, Report SOC-151, 1977.

[9] E.M. Butler, "Techniques for statistical DC modeling of bipolar transistors", Proc. 1974 IEEE Symp. on Circuits and Systems (San Francisco, CA, April 1974), pp. 725-729.

[10] H.L. Abdel-Malek and J.W. Bandler, "Yield optimization for arbitrary statistical distributions, Part II: Implementation", Faculty of Engineering, McMaster University, Hamilton, Canada, Report SOC-185, 1977.

TABLE I(a)
CIRCUIT PARAMETER VALUES

R_1	281.33 Ω	E_2	4.03 V
R_2	75.00 Ω	E_3	1.13 V
R_3	78.24 Ω	E_4	1.70 V
R_4	50.00 Ω	C_0	1.50 pF

TABLE I(b)
DIODE MODEL PARAMETERS

I_{SD}	diode saturation current	0.6×10^{-9} A
C_{JD}	depletion layer capacitance	0.12 pF
TT_D	transit time	0.01 ns
θ	inverse of thermal potential	38.668 V^{-1}

$I_D = I_{SD}(\exp(\theta V_D)-1)$, $C_D = C_{JD} + TT_D\ (dI_D/dV_D)$

TABLE II
WORST-CASE DESIGN FOR THE CSEF CIRCUIT

E_4^0 (V)	Z_0^0 (Ω)	R_4^0 (Ω)	C_0^0 (pF)	ϵ_1/E_4^0 (%)	ϵ_2/Z_0^0 (%)	ϵ_3/R_4^0 (%)	ϵ_4/C_0^0 (%)
1.66	92.00	45.53	1.25	4.5	8.3	13.8	14.0

Number of complete response evaluations = 30

CDC modeling time = 48 s

CDC time (approximation and optimization) = 103 s

TABLE I(c)
TRANSISTOR MODEL PARAMETERS

I_S	saturation current	0.6×10^{-9} A
α	common base current gain	0.99
R_B	base resistance	50.0 Ω
C_C	collector junction capacitance	0.5 pF
C_{JE}	emitter junction depletion layer capacitance	0.12 pF
TT	base transit time	0.01 ns
θ	inverse of thermal potential	38.668 V^{-1}

$I_E = I_S(\exp(\theta V_{BE})-1)$, $I_C = \alpha\ I_E$, $C_E = C_{JE} + TT\ \frac{dI_E}{dV_{BE}}$

R_B and C_C are assumed zero for transistor T_3

TABLE I(d)
TRANSMISSION-LINE PARAMETERS

Z_0	characteristic impedance	50 Ω
τ	delay time	0.25 ns

TABLE III
RESULTING WEIGHTS DUE TO CORRELATION BETWEEN β, I_S and C_{JE}

β		α*		I_S			C_{JE}		
ϵ_{β,i_β}	w	$\epsilon_{\alpha,i_\alpha}$	w	w_1	w_2	w_3	w_1	w_2	w_3
20.0	0.3333	0.0080	0.3333	0.8320	0.1680	0.0000	0.2345	0.4084	0.3571
20.0	0.5000	0.0041	0.5000	0.3599	0.6113	0.0288	0.3174	0.4258	0.2568
20.0	0.1667	0.0024	0.1667	0.0744	0.5731	0.3525	0.4059	0.4472	0.1469

*$\alpha = \beta/(\beta+1)$

Equal intervals for I_S of $\epsilon_{I_S,i} = 0.221 \times 10^{-9}$ A and for C_{JE} of $\epsilon_{C_{JE},i} = 0.0218$ pF are considered

Lower extremes of the parameters are β = 40.0, α = 0.9756, $I_S = 0.1582 \times 10^{-9}$ A and $C_{JE} = 0.0958$ pF

TABLE IV
INTERPOLATION REGION SIZE AND CENTER FOR THE CSEF EXAMPLE

	E_4 (V)	Z_0 (Ω)	R_4 (Ω)	C_0 (pF)	α_3	I_{S3} (10^{-9} A)	C_{JE3} (pF)	TT_3 (ns)
$\bar{\phi}$	1.632	95.0	44.0	1.35	0.98285	0.49135	0.1285	0.0100
$\underset{\sim}{\delta}$	0.170	15.0	10.0	0.45	0.00786	0.34400	0.0380	0.0025

TABLE V
RESULTS FOR THE MAXIMIZATION OF YIELD
FOR THE CSEF CIRCUIT

	E_4^0 (V)	Z_0^0 (Ω)	R_4^0 (Ω)	C_0^0 (pF)	Opt. time (sec)	Yield (%) Linear cut	Yield (%) M.C.
Start	1.632	95.0	44.00	1.35	-	25.7	39.4
Optimum $Z_{0u}=100\Omega$	1.595	100.0	51.15	1.27	67.8	58.6	68.9
Optimum $Z_{0u}=105\Omega$	1.638	105.0	53.07	1.27	40.6	85.6	89.1

CDC modeling time = 74 s

CDC time for M.C. employing approximation ≃ 5 s

TABLE VI
YIELD OPTIMIZATION FOR DIFFERENT SPECIFICATIONS

Specifications a	Specifications b	E_4^0 (V)	Z_0^0 (Ω)	R_4^0 (Ω)	C_0^0 (pF)	Yield (%) Linear cut
-1.450	-0.900	1.657	90.0	51.84	1.27	65.1
-1.425	-0.925	1.652	90.0	48.95	1.27	91.4
-1.400	-0.950	1.637	90.0	44.91	1.27	99.7

$V_0(t) \leq a$ V, t = 0.3, 1.02, 1.09, 1.2 ns

$V_0(t) \geq b$ V, t = 0.62, 0.69, 0.8 ns

$Z_{0u} = 90\Omega$

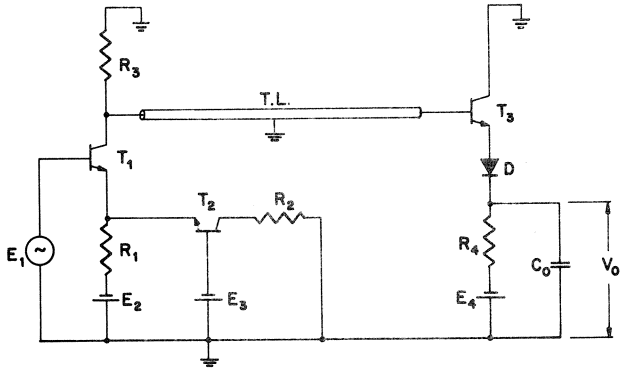

Fig. 1 The CSEF circuit[4].

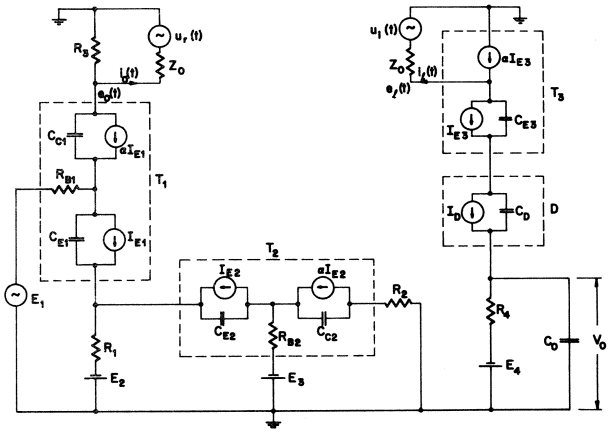

Fig. 2 The CSEF circuit used, indicating transmission-line, transistor and diode models.

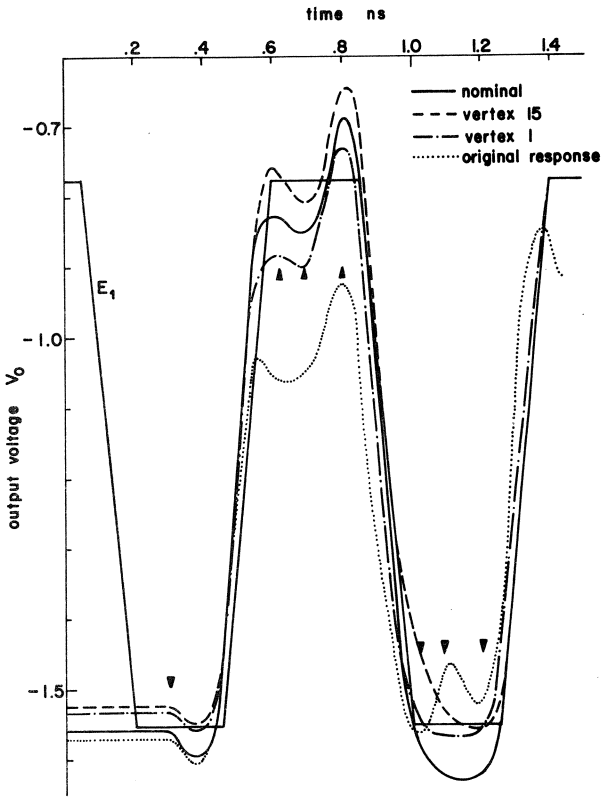

Fig. 3 Original, nominal and worst-case responses of the CSEF.