ANALYTICALLY UNIFIED
DC/SMALL-SIGNAL/LARGE-SIGNAL CIRCUIT DESIGN

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ABSTRACT

We unify DC, small-signal and large-signal circuit design concepts and techniques. Circuits are optimized to simultaneously meet DC/small-signal/large-signal specifications. Unified FET model parameter extraction provides consistent bias dependent device models suitable for both small- and large-signal simulations. In a FET broadband amplifier design example the dynamic operating range is extended. Optimization of bias circuits is illustrated.

INTRODUCTION

This paper demonstrates the analytical relationship between small-signal analysis and harmonic balance (HB) analysis for sufficiently small input signals (HBSS). The circuit design problem is proved to converge to a single unified optimization problem, which, we believe, must be a distinctive feature of the next generation of microwave CAD software. Consistent device models can then be used and other factors affecting the behaviour of circuits such as bias, temperature, etc., can be simultaneously taken into account during optimization.

Examples demonstrate that consistent results can be reached which meet design specifications for both large and small signals. Our approach offers superior results w.r.t. those obtained by considering small- and large-signal operations independently from each other.

CONSISTENCY OF DC/SMALL-SIGNAL/LARGE-SIGNAL ANALYSIS

We use the same notation as in [1]. Boldface letters are used to indicate vectors or matrices, and superscript T denotes transposition.

Assume that the HB equation for a nonlinear circuit is

$$F(V) = I(V) + j\Omega Q(V) + YV + I_s = 0 , \qquad (1)$$

where $V = [V^T(0) \quad V^T(1) \quad ... \quad V^T(H)]^T$ is the variable vector to be solved for, usually the node voltages at the nodes connecting the linear and nonlinear parts of the circuit, H is the number of harmonics considered in the simulation, $I(V)$ represents the current of nonlinear resistive elements and voltage controlled nonlinear current sources in the circuit, $Q(V)$ the charges of nonlinear capacitors, $\Omega = \text{diag}\{\Omega(0), \Omega(1), ..., \Omega(H)\}$ with $\Omega(k) = \text{diag}\{\omega_k, \omega_k, ..., \omega_k\}$ and ω_k the kth harmonic frequency in radians, Y is the admittance matrix describing the linear part of the circuit, and I_s contains the equivalent current excitation sources.

Using Fourier series, we have

$$v(t) = \sum_{\ell=-H}^{H} V(\ell)e^{j\ell\omega_o t}.$$

The time invariant and variant parts can be briefly expressed as

$$v(t) = V(0) + \Delta v(t) . \qquad (2)$$

Let the current of nonlinear resistive elements and voltage controlled nonlinear current sources in the time domain be $i(v(t))$. It can be shown that under small-signal operation, i.e., $\Delta v(t) \approx 0$,

$$\frac{\partial I^T(V,k)}{\partial V(m)} = \frac{1}{T_0} \int_0^{T_0} \frac{\partial i^T(v(t))}{\partial v(t)} e^{jm\omega_o t} e^{-jk\omega_o t} \, dt$$

$$\approx \begin{cases} \left. \dfrac{\partial i^T(v(t))}{\partial v(t)} \right|_{V(0)} & k=m, \; k,m = 0,1, ..., H \\ \\ 0 & k \neq m, \; k,m = 0,1, ..., H \end{cases}$$

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Similar derivations can be applied to Q(V). Therefore, under small-signal conditions, the Jacobian matrix of (1) tends to be block diagonal. From the Newton iteration method, it is not difficult to derive that (1) can be solved by first solving the nonlinear equation

$$F(V(0)) = I(V(0)) + Y(0)V(0) + I_s(0) = 0 \qquad (3)$$

and then a set of linear equations

$$\left\{ \left[\frac{\partial I^T(V,k)}{\partial V(k)} \right]^T_{V(0)} + j\Omega(k) \left[\frac{\partial Q^T(V,k)}{\partial V(k)} \right]^T_{V(0)} + Y(k) \right\} V(k)$$

$$+ I_s(k) = 0 \qquad k=1,...,H, \qquad (4)$$

where V(0) is the solution of (3).

Equations (3) and (4) verify that DC/small-signal circuit analysis is a special case of HB analysis. This leads to a specialized HB technique for small-signal analysis which we call HBSS. It should be emphasized, however, that while there exist techniques for DC/ small-signal simulation that do not require explicit AC excitations, an AC excitation is indispensable to HBSS simulation.

SEAMLESS DC/SMALL-SIGNAL/LARGE-SIGNAL CIRCUIT DESIGN AND OPTIMIZATION

Using the consistency between DC/small-signal/ large-signal analysis, general circuit design can be formulated into one optimization problem with error functions consisting of $e_{dc}(\phi)$, $e_{ss}(\phi)$ and $e_{ls}(\phi)$ from DC, small-signal and large-signal domain, respectively, where ϕ represents circuit optimization variables common to DC, small-signal and large-signal circuits. Because of our unification, ϕ can include not only usual variables such as resistors, capacitors, FET parameters, and so on, but also other parameters such as bias voltages.

CAD systems, such as Libra [2] and Microwave Harmonica [3], have adopted simulation with uncoupled DC, small-signal and large-signal analyses. For combined specifications, manual manipulations have to be involved.

EXAMPLES

Both parameter extraction and design optimization examples are presented employing the McCAE research software system.

Example 1   We extract FET model parameters by simultaneously matching DC, small-signal and large-signal measurements [4,5]. The circuit diagram is shown in Fig. 1 with the Curtice nonlinear FET model [6]. Totally, 27 variables are considered, including all parameters in the intrinsic FET model and all elements in the extrinsic circuit.

Measurement sets used are listed in Table I. Error functions e_{dc} represents the 2 errors between measured and modeled DC drain bias currents, e_{ss} the 128 errors

between measured and modeled S-parameters, and e_{ls} the 48 errors between measured and modeled harmonic output powers. Least-squares optimization is applied to simultaneously minimize those 178 error functions. From the same initial guess of parameter values two parameter extractions were performed by matching (1) large-signal measurements only, and (2) DC, small-signal and large-signal measurements simultaneously.
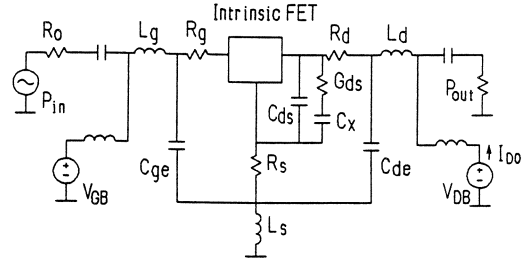

Fig. 1   Single FET circuit with the Curtice nonlinear intrinsic FET model.

TABLE I

MEASUREMENT SETS FOR EXAMPLE 1

DC measurements	
Response type	drain current
Bias conditions	V_{GB}=-0.361V V_{DB}=2V V_{GB}=-1.062V V_{DB}=6V

Small-signal measurements	
Response types	magnitudes and phases of 4 S-parameters
Bias conditions	V_{GB}=-0.361V V_{DB}=2V V_{GB}=-1.062V V_{DB}=6V
Frequencies (GHz)	1, 3, 5, 7, 9, 11, 13, 15

Large-signal measurements	
Response types	DC drain current, output powers at the fundamental, second and third harmonics
Bias conditions	V_{GB}=-0.373V V_{DB}=2V V_{GB}=-1.072V V_{DB}=6V
Input power (dBm)	-15, -5, 5
Fundamental frequencies (GHz)	0.2, 6

Fig. 2 illustrates the match in large-signal responses at solutions reached by the two different approaches. A bias-fundamental frequency point not used in the optimization is selected to illustrate the model prediction. Both give reasonably good matches. However, for small-signal S-parameter matches, as shown in Fig. 3, very good agreement is observed at the solution obtained by simultaneous DC/small-signal/large-signal optimization, yielding considerable improvement over the results by matching large-signal data alone.

Example 2 We design a small-signal broadband amplifier [7]. The circuit diagram is shown in Fig. 4, where the FET model is taken from the result of Example 1. We assume the specifications for the amplifier to be

$$\text{GAIN} = 8 \pm 0.5\text{dB}$$
$$|S_{11}| \leq 0.4$$
$$|S_{22}| \leq 0.4$$
$$|S_{12}| \leq 0.15$$

at frequencies 4, 5, 6, 7 and 8GHz. The design variables are 11 element parameters in the matching network and 2 resistor values in the bias network. Minimax optimization [8] is used.

First, we design the amplifier by the conventional small-signal approach at a predetermined bias point selected approximately in the middle of the FET DC I-V curve. All the specifications can be met at the optimal solution under small-signal conditions. Then, we exploit our new design strategy to include the dynamic range of the amplifier in addition to the small-signal specifications. Specifically, we add specifications to extend the gain of the amplifier at input available power levels -10, -5 and 0dBm, and enforce second and third harmonic output power levels to be at least 40dB below the fundamental output power level. All small- and large-signal specifications result in 85 error functions. We also allow the bias circuits to be optimized. All small-signal/large-signal specifications are met at the solution.

At the solution the gain response surfaces are depicted in Fig. 5 over fundamental frequency 2 to 10GHz and input available power -35 to 5dBm. It can be seen that the gain surface in Fig. 5(b) is flatter and provides a wider area which meets the gain specification.

CONCLUSIONS

We present a unified theory to simultaneously optimize DC, small-signal and large-signal performance. Our approach has the following distinctions.
(1) The inherent consistency of small- and large-signal analyses and unified optimization guarantees designs which simultaneously meet DC/small-signal/large-signal specifications.
(2) A much wider range of design variable selections is permitted. Besides linear elements, design variables can include nonlinear elements, controllable operating parameters, such as bias, and possibly process parameters. Therefore, the nonlinearity of the circuit at different levels can be effectively exploited.
(3) Design specifications can be expanded from the traditional frequency dimension into a multidimensional space [9]. For example, specifications can be imposed at different input power levels in a small-signal circuit design to increase the dynamic operating range.

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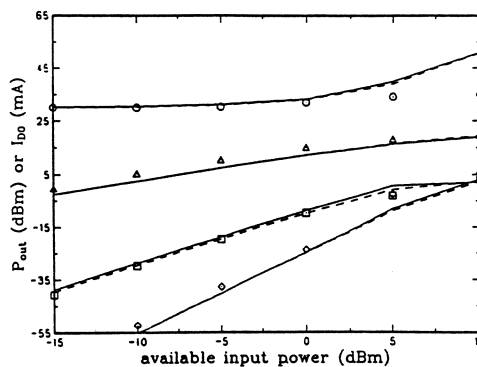
Fig. 2 Agreement between model responses and large-signal measurements at fundamental frequency 2GHz and bias $V_{GB}=-0.667V$ and $V_{DB}=4V$. Solid lines represent responses of the model extracted from both small- and large-signal matching. Dashed lines represent responses of the model extracted only from large-signal fitting. Circles, triangles, squares, and diamonds stand for DC, fundamental, second, and third harmonic measurements, respectively.
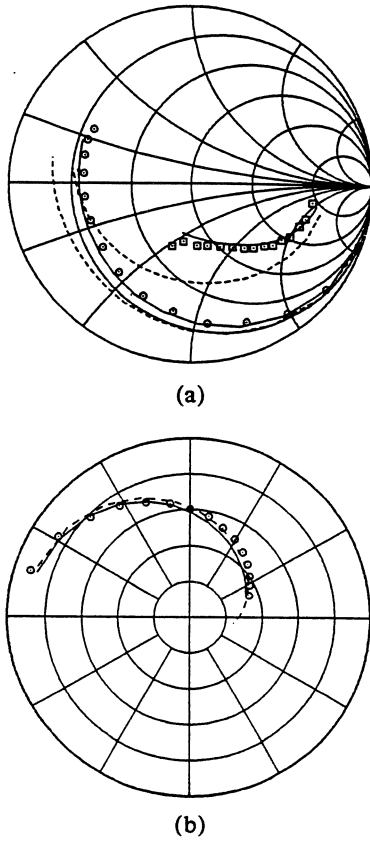
(a)

(b)

Fig. 3 Agreement between model responses and S-parameter measurements at bias V_{GB}=-0.667V and V_{DB}=4V. Solid lines represent responses of the model determined from both small- and large-signal matching. Dashed lines represent responses of the model determined only from large-signal fitting. (a) S_{11} and S_{22} fitting, where circles and squares represent S_{11} and S_{22} measurements, respectively. (b) S_{21} fitting, where circles are from S_{21} data.
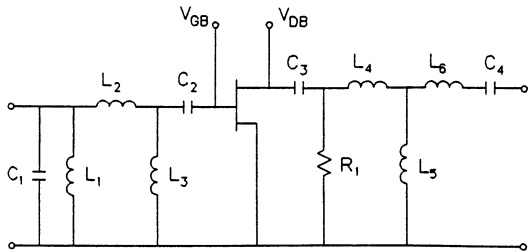

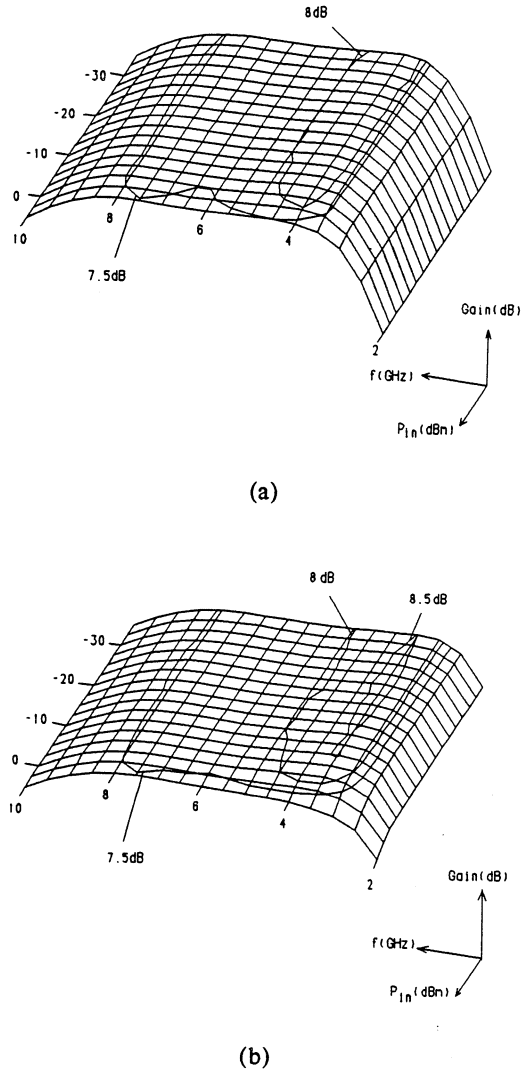Fig. 4 4-8GHz broadband small-signal amplifier.

(a)

(b)

Fig. 5 (a) The gain response surface simulated at the solution obtained by small-signal design. (b) The gain response surface simulated at the solution obtained by simultaneous small- and large-signal design. Contours indicate the specification of 8±0.5dB.