PREDICTABLE YIELD-DRIVEN CIRCUIT OPTIMIZATION

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ABSTRACT

This paper presents a comprehensive approach to predictable yield optimization. We utilize a new physics-based statistical GaAs MESFET model which combines the advantages of the dc Khatibzadeh and Trew model and the small-signal Ladbrooke formulas. The yield of a broadband amplifier is significantly improved after optimization. Predicted yield over a range of specifications is verified by device data. The benefits of simultaneous circuit-device yield optimization assisted by yield sensitivity analysis are demonstrated.

INTRODUCTION

The practical usefulness of microwave circuit yield optimization [1-3] depends on the accuracy of the statistical models and the predictability of the design yield. We present in this paper a comprehensive approach to predictable yield-driven physics-based circuit optimization.

We promote physics-based models (PBMs) because they allow characterization of device statistics at the geometrical/process parameter level. For a given process, the nominal values of some physical parameters as well as their probable ranges of deviations may be known, providing reliable information for statistical modeling.

We present a new MESFET PBM which combines the advantages of the Khatibzadeh and Trew model [4] and the small-signal Ladbrooke formulas [5] while overcoming their respective shortcomings: the dc operating point for the Ladbrooke model has to be obtained separately; the Khatibzadeh and Trew model, while capable of dc simulation, seems to be inaccurate for small-signal statistical applications. The statistics of the model parameters are extracted from statistical (multi-device) measurement data.

To demonstrate for the first time that yield predicted by Monte Carlo simulation using a PBM can be consistent with yield predicted directly from device data, we performed yield optimization of a broadband small-signal amplifier using OSA90/hope™ [6] and obtained convincing results.

This work was supported in part by Optimization Systems Associates Inc. and in part by the Natural Sciences and Engineering Research Council of Canada under Grants OGP0007239, OGP0042444 and STR0040923.

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Representing devices by PBMs instead of using measured S parameters directly has an advantage: the model can interpolate device behaviour at frequency and bias points not contained in the data. The use of PBMs also presents us with the opportunity of optimizing the active devices. Although device optimization can be expensive to implement, it may be justified if it significantly increases the yield and therefore reduces the production cost. Device optimization may also become more attractive with further advances in technology.

We demonstrate the benefits of simultaneous circuit and device optimization by showing that a significantly higher yield can be achieved by including suitable FET parameters such as the gate length and channel thickness as design variables. The selection of device parameters for yield optimization can be assisted by yield sensitivity analyses.

STATISTICAL GaAs MESFET MODEL

We created a new physics-based MESFET model which combines the advantages of the Khatibzadeh and Trew model [4] and the Ladbrooke model [5]. It includes our modifications to the Khatibzadeh and Trew model for better efficiency under uniform doping [6]. This model is used to solve the nonlinear circuit for the dc operating point. At the dc operating point, the small-signal equivalent circuit is derived from device geometrical/process parameters and the dc intrinsic voltages using the Ladbrooke formulas with our modifications [7].

The model includes the intrinsic parameters

$$\{L, Z, a, N_d, V_{b0}, v_{sat}, E_c, \mu_0, \varepsilon, L_{G0}, a_0, r_{01}, r_{02}, r_{03}\}$$

and the linear extrinsic elements

$$\{L_g, R_g, L_d, R_d, L_s, R_s, G_{ds}, C_{ds}, C_{ge}, C_{de}\}$$

where L is the gate length, Z the gate width, a the channel thickness, N_d the doping density, V_{b0} the zero-bias barrier potential, v_{sat} the saturation value of electron drift velocity, E_c the critical electric field, μ_0 the low-field mobility of GaAs, ε the dielectric constant, L_{G0} the inductance from gate bond wires and pads, a_0 the proportionality coefficient, and r_{01}, r_{02} and r_{03} are fitting coefficients [7].

The device statistics are represented by a multidimensional statistical model. The mean values, standard deviations, correlation coefficients and discrete distribution functions [8] of the parameters are extracted from wafer measurements provided by Plessey Research Caswell [9]. Measured dc and S-parameter data for 69 devices were used. The multi-device parameter extraction and postprocessing of the statistical model were accomplished using HarPE™ [10]. The parameter values and statistics are listed in Table I.

TABLE I

MESFET MODEL PARAMETERS

Parameter	Mean	Standard Deviation (%)
$L(\mu m)$	0.4997	4.76
$a(\mu m)$	0.1630	5.78
$N_d(m^{-3})$	2.475×10^{23}	4.21
$V_{b0}(V)$	0.2661	34.6
$L_{G0}(nH)$	0.0299	9.02
$r_{01}(1/A^2)$	0.0779	0.17
$r_{02}(V)$	534.44	4.86
$r_{03}(\Omega)$	7.7855	0.17
$R_d(\Omega)$	0.4905	1.42
$R_s(\Omega)$	3.9345	1.29
$R_g(\Omega)$	7.7811	0.34
$L_d(nH)$	6.21×10^{-2}	5.88
$L_s(nH)$	2.15×10^{-2}	7.31
$G_{ds}(1/\Omega)$	2.34×10^{-3}	4.19
$C_{ds}(pF)$	5.89×10^{-2}	2.33
$C_{ge}(pF)$	4.61×10^{-2}	6.12
$C_{de}(pF)$	2.00×10^{-4}	0.05
$Z(\mu m)$	300	*
$v_{sat}(m/s)$	9.5×10^{4}	*
$E_c(V/m)$	1.9×10^{5}	*
$\mu_0(m^2/Vns)$	5×10^{-10}	*
ε	12.5	*
a_0	1.0	*

* Assumed fixed (non-statistical) parameters. The linear extrinsic element L_g is computed by the Ladbrooke formulas [5,7].

YIELD OPTIMIZATION

We consider the small-signal broadband amplifier shown in Fig. 1.

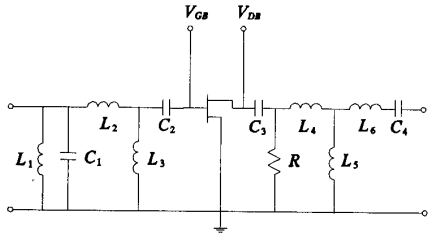


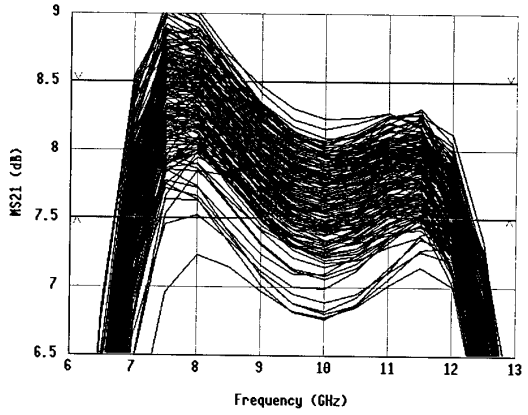
Fig. 1. Small-signal broadband amplifier.

The specifications for yield optimization are: $|S_{21}|$ = 8dB ± 0.5dB, $|S_{11}| < 0.5$ and $|S_{22}| < 0.5$ for the frequency range 8GHz-12GHz. The matching network elements, namely, L_1, L_2, L_3, L_4, L_5, L_6, C_1, C_2, C_3, C_4 and R, are chosen as design variables. They are also assigned random variations of uniform distribution with a 5% tolerance. Adding these to the FET parameters, we have a total of 28 statistical variables. The optimization was carried out using OSA90/hope [6] on a Sun SPARCstation 1.

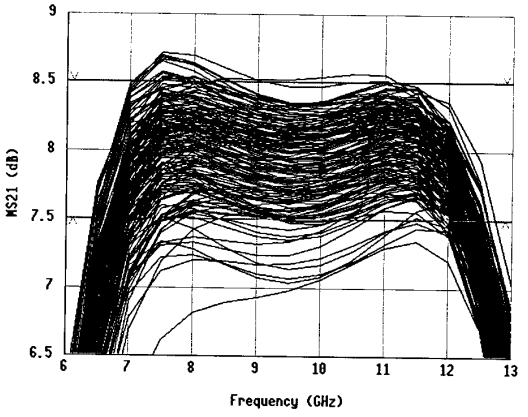
First, a nominal minimax design was obtained (after 133 iterations and about 12 minutes CPU time). The yield of the nominal design is estimated as 17.5% by Monte Carlo simulation with 200 outcomes.

Using the nominal design as the starting point, yield optimization was performed with 100 outcomes. After 30 iterations (145 minutes CPU time), the yield was increased to 67% as estimated by Monte Carlo simulation with 200 outcomes.

The Monte Carlo sweeps of $|S_{21}|$ before and after yield optimization are shown in Fig. 2. Table II lists the values of the design variables before and after yield optimization.



(a)



(b)

Fig. 2. Monte Carlo sweeps of $|S_{21}|$ using the statistical PBM, (a) before yield optimization and (b) after yield optimization.

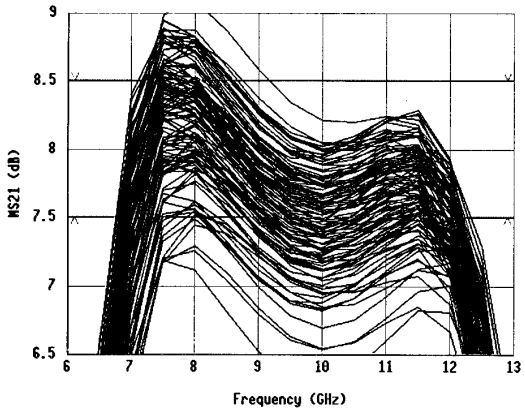
YIELD VERIFICATION

The significance of yield optimization will be much more convincing if the yield predicted by statistical models can be shown to be consistent with actual device data. To demonstrate that this indeed can be the case, we substitute the FET model with device data and compare the Monte Carlo yields for both cases. Because the wafer measurements contain small variations in bias conditions between different devices, we use the Materka and Kacprzak model [11] to interpolate individual device data at the same bias point (V_{GB}=-0.7V and V_{DB}=5V).

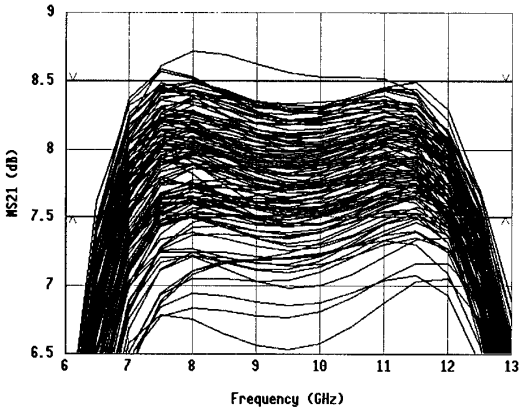
TABLE II

MATCHING CIRCUIT OPTIMIZATION

Design Variable	Before Yield Optimization	After Yield Optimization
C_1(pF)	0.6161	0.4372
C_2(pF)	5.2556	6.1365
C_3(pF)	0.2606	0.2757
C_4(pF)	0.1385	0.1570
R(Ω)	589.00	708.08
L_1(nH)	0.5947	0.9110
L_2(nH)	0.9916	0.9430
L_3(nH)	1.9203	1.6395
L_4(nH)	1.5754	1.7516
L_5(nH)	2.0039	2.3933
L_6(nH)	1.0085	0.7537



(a)



(b)

Fig. 3. Monte Carlo sweeps of $|S_{21}|$ using device data (140 outcomes), (a) before yield optimization and (b) after yield optimization.

The yield predicted by Monte Carlo simulation using the device data and 140 outcomes was 15.7% (nominal design) and 57.9% (after yield optimization). This verifies very well the yields predicted by our nonlinear statistical model (which are 17.5% and 67%, respectively). The Monte Carlo sweeps of $|S_{21}|$ using the device data are shown in Fig. 3, which are in excellent agreement with those produced by the statistical model (Fig. 2).

To show that the good result is not a singular exception, we varied the design specifications over a range and applied the same procedure. As shown in Table III, the yields predicted by the model and the device data are in very good agreement in all cases.

TABLE III

YIELD PREDICTED BY MODEL AND VERIFIED BY DATA

	Before Yield Optimization		After Yield Optimization	
Specification	Predicted Yield (%)	Verified Yield (%)	Predicted Yield (%)	Verified Yield (%)
Spec. 1	17.5	15.7	67	57.9
Spec. 2	21	20	83	75.7
Spec. 3	44	37.1	98	93.6

Spec. 1: 7.5dB < $|S_{21}|$ < 8.5dB, $|S_{11}|$ < 0.5, $|S_{22}|$ < 0.5.
Spec. 2: 6.5dB < $|S_{21}|$ < 7.5dB, $|S_{11}|$ < 0.5, $|S_{22}|$ < 0.5.
Spec. 3: 6.0dB < $|S_{21}|$ < 8.0dB, $|S_{11}|$ < 0.5, $|S_{22}|$ < 0.5.

200 outcomes are used for yield prediction by the statistical PBM, 140 for yield verification using the device data.

YIELD SENSITIVITY ANALYSIS

Yield is a function of device parameters, circuit elements, parameter statistics and design specifications. To select a proper set of variables for yield optimization can be a delicate task. We use OSA90/hope to calculate the sensitivities of yield w.r.t. circuit and design parameters. This analysis reveals the influence of different parameters on yield, and this information can assist us in selecting variables for yield optimization.

To illustrate, we performed yield sensitivity analysis w.r.t. two parameters which were not included in the optimization of the matching network, namely, one design specification and one device parameter (the FET gate length).

Fig. 4 depicts the yield sensitivity w.r.t. the lower specification on the gain (the upper specification was fixed). It shows, for instance, that if the lower specification is relaxed from 7.5dB to 7.3dB, the yield would increase from 67% to 74.5%. Fig. 5 depicts the yield sensitivity w.r.t. the FET gate length. It clearly shows that the gate length has a strong influence on yield and therefore merits inclusion as a variable for yield optimization.

SIMULTANEOUS DEVICE-CIRCUIT DESIGN

Physics-based models (PBMs) provide an opportunity for designers to optimize the geometrical and process parameters of active devices, which is not possible if the devices are represented by *S* parameters. Although device optimization can be expensive

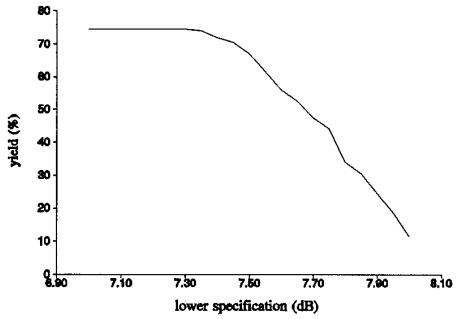


Fig. 4. Yield versus the lower specification on the gain.

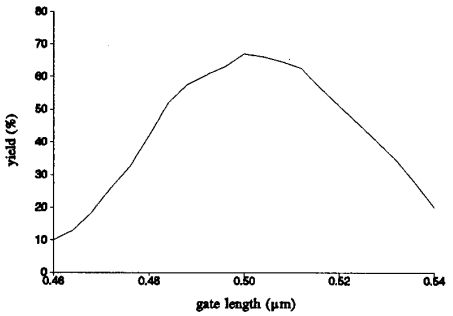


Fig. 5. Yield versus the FET gate length.

to implement, it may be justified when stringent specifications result in very low yield which cannot be sufficiently improved by optimizing the matching circuit alone.

Consider again the small-signal broadband amplifier. We tighten the upper specification on $|S_{11}|$ from 0.5 to 0.4 in the passband, while the other specifications remain the same. Two separate cases of optimization were constructed as follows. In Case I, only the matching circuits are optimized. In Case II, we include the GaAs MESFET gate length and channel thickness as design variables in addition to the matching circuits.

In both cases, we first performed a minimax nominal optimization and then a yield optimization. In Case I, at the nominal solution the yield predicted by Monte Carlo simulation using 200 outcomes is only 7.5%. After yield optimization the yield is improved to 27.5%.

In Case II, the yield at the nominal solution is 12.5%, and is increased to 64.5% after yield optimization. Compared with Case I, this drastic improvement in the optimized yield requires relatively small changes in the device parameters: the gate length changed from 0.5μm to 0.4μm and the channel thickness from 0.163μm to 0.14μm.

CONCLUSIONS

A comprehensive approach to yield-driven optimization has been presented. We have addressed various stages of yield-driven CAD: statistical modeling, nominal design optimization, yield optimization, yield verification and device optimization.

Through a broadband small-signal amplifier, we have demonstrated for the first time predictable yield optimization using physics-based models. Excellent agreement has been shown between the yield estimated by the statistical model and the yield verified through device data.

Simultaneous device and circuit optimization assisted by yield sensitivity analyses further champions the relevance and benefits of our physics-based technique for MMICs. We believe that device optimization will become more attractive with continuing advances in technology.

ACKNOWLEDGEMENTS

The authors thank Dr. D.M. Brookbanks for technical discussions and providing the measurement data [9].

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