Signal Integrity Optimization of High-Speed VLSI Packages and Interconnects

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Abstract

Signal integrity of high-speed VLSI packages and interconnects is becoming one of the critical issues in an overall system design as the operating frequency in electronic systems such as computers and digital communication systems is going higher and higher. In recent years, research into the VLSI package and interconnect optimization problems has been very active, and several important progresses have been made. This paper presents the review of recent development in signal integrity oriented optimization of VLSI packages and interconnects. Advanced optimization techniques are also presented with emphasis on large scale optimization and space mapping, a new concept linking engineering models of different types and levels of complexity.

Introduction

As the operating frequency in electronic systems such as computers and digital communication systems becomes higher and higher, VLSI interconnects (Figure 1) are becoming more and more critical in an overall system design. The overall system performance could be affected by improperly designed interconnects because of signal integrity degradations such as signal delay, crosstalk and ground noise.

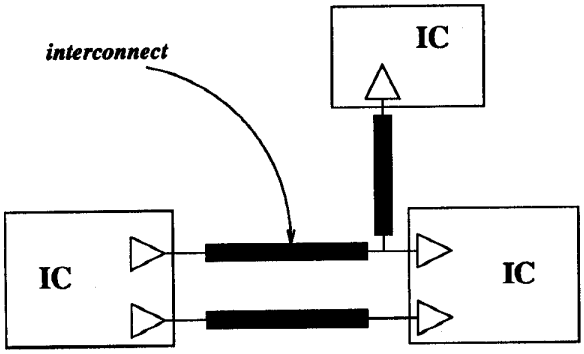

Figure 1. VLSI interconnect network with driver and receiver terminations.

Practical circuit boards usually have a large number of interconnects and various design criteria. At the same time, there is an increasing need that the signal integrity criteria be directly used in interconnect design optimization [1][2][3][4]. An overall optimization of various signal performances can become very complicated in this case. The problem is often large scale optimization by nature [5] , and can involve highly repetitive simulation of distributed transmission line models or even EM models [6]. Straight use of conventional circuit optimization approaches will not always be suitable. The hierarchical nature of signal integrity at chip, multichip module (MCM), printed circuit board (PCB) levels also poses challenges [6]. In addition, electrical design is now more and more constrained by other design factors such as thermal [7] and Electromagnetic (EM) effects [8], both of which are becoming important considerations in an overall design.

In recent years, research into the high-speed VLSI package and interconnect optimization problems has been very active, and several important progresses have been made. This paper summarizes the current status of the subject area.

Objectives of Signal Integrity Oriented Optimization

A direct signal integrity oriented optimization can be performed in the time-domain [1] with error functions based on the performances of transient responses such as delay, rise/fall times, crosstalk and reflection, such as those listed in Table I. Another type of important design objective in the time-domain is skew reduction [4][5], which is to minimize the difference of the delay at several signal paths. Alternatively, the optimization can also be performed indirectly in the frequency domain. Different objectives have been used. Group delay contains information of signal propagation delay. By reducing group delay and spectrum of crosstalks, and improving the flatness of group delay and gain slope responses, the transient signal delay, crosstalk and signal distortions are indirectly optimized [2]. Elmore delay, which is equivalent to 1st order moment of the delay function, has been used as an approximate measure for delay reduction at chip level using lumped interconnect model [9]. In general cases, higher order moments can be used [10]. Moments up to 3rd order have been used to characterize the signal behaviour of distributed transmission lines [10] such that optimization in the frequency domain can be formulated without time domain simulations. In an overall design task, the frequency-domain approach can be used in the initial design stage to achieve a near-optimal design. The time-domain approach can be used in the final design stage for verification and fine tuning.

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Performance	Error Functions
propagation delay	$w_d(v_j(\Phi,\tau_j)-v_T)$ $-w_d(v_j(\Phi,\tau_j)-v_T)$ *for* $j\in \mathbf{J}_1$
rise time	$w_f(v_j(\Phi,\tau_j-\alpha t_r)-v_{T,low})$ $-w_f(v_j(\Phi,\tau_j+\beta t_r)-v_{T,high})$ *for* $j\in \mathbf{J}_1$ where α and β are positive and $\alpha+\beta=1$
fall time	$w_f(v_j(\Phi,\tau_j+T+\lambda t_f)-v_{T,low})$ $-w_f(v_j(\Phi,\tau_j+T-\mu t_f)-v_{T,high})$ *for* $j\in \mathbf{J}_1$ where λ and μ are positive and $\lambda+\mu=1$
crosstalk	$w_c(t)(v_j(\Phi,t_i)-S_{cj}(t_i))$ $-w_c(t)(v_j(\Phi,t_i)+S_{cj}(t_i))$ *for* $j\in \mathbf{J}_2$ and $0<t_i<\infty$
reflections	$w_r(t)(v_j(\Phi,t_i)-S_{rj}(t_i))$ $-w_r(t)(v_j(\Phi,t_i)+S_{rj}(t_i))$ *for* $j\in \mathbf{J}_1$ and $T+\tau_j+\delta<t_i<\infty$

where τ_j, S_{cj} and S_{rj} are upper specifications for delay, crosstalk and reflection at node j, respectively; t_r and t_f are required rise/fall times, respectively; $V_T, V_{T,low}$ and $V_{T,high}$ are threshold voltages for measuring delay and rise/fall times.

Table I. Error functions for time-domain signal integrity optimization.

Advanced Optimization Techniques

An approach to speed up simulation for use in either frequency- or time-domain based interconnect optimization is to exploit parallel computation [11]. The frequency-domain case has an inherent parallel feature because the circuit response at one frequency point is independent of those at other frequency points. Parallel computation in the time-domain optimization is not applicable for conventional simulation techniques. In [11], a specific simulation technique based on numerical inversion of Laplace tranmiform (NILT), is used to simulate signal waveforms with parallel simulation. A multilevel approach taking advantage of network topological decomposition as well as optimization decomposition is another development [5]. The overall optimization is reformulated to yield a set of independent suboptimization problems that are solved by parallel processing. The suboptimizations are coordinated by a model coordinating scheme. This formulation fits well with a VLSI system in which the PCB interconnect circuitry is optimized by the high-level optimization and several MCM's are optimized at the low level.

An important recent development is neural network technology applied to interconnect optimization [12]. Neural network models can be used at different levels of the interconnect problem inside the optimization cycle, i.e., Physical/EM level or circuit level. The model is trained off-line from sample data and used during optimization for fast evaluation of signal integrity with its generalization property, i.e., predicting the outputs upon the given input information that may not have been seen during training.

Another totally new concept in engineering optimization is Space Mapping (SM) [13]-[21], linking engineering models of different types and levels of complexity, including empirical, EM-based, analytical, numerical, physics based, and even direct laboratory measurements, which represent the same physical design. With today's signal integrity requirments, interconnects are more modeled with EM effects [17]. The application of space mapping with signal integrity design of VLSI packages and interconnects has significant effect in speeding up the optimization process.

A key step in SM is to determine pairs of corresponding EM and empirical models through parameter extraction. In its basic form, the SM optimization technique [13][14] exploits a mathematical link between input parameters of two simulators (models). One is considered very accurate but computationally very intensive, the other one is fast but less accurate. The goal is to direct the bulk of CPU-intensive optimization to the fast model in the optimization system (OS) parameter space X_{OS}. This model is referred to as the OS simulator. EM simulations serve as the accurate model and the EM simulator input parameter space is denoted by X_{EM}. As a first step in SM optimization we carry out conventional design optimization entirely in the X_{OS} space. The resulting solution is denoted by x^*_{OS}. Then we create and iteratively refine a mapping

$$x_{OS} = P(x_{EM}) \qquad (1)$$

from X_{EM} to X_{OS} in order to align the two models. In [13] the mapping was assumed to be expressed as a linear combination of some predefined and fixed fundamental functions. In the current implementation of SM [14][19], P is also assumed invertible. Once the mapping is established the inverse mapping P^{-1} is used to find the EM solution as the image of the optimal OS solution x^*_{OS}, namely,

$$x^*_{EM} = P^{-1}(x^*_{OS}) \qquad (2)$$

In other words, we map the optimal OS model parameters back into the EM parameters. P is established through an iterative process to satisfy the constraint that

$$f_{OS}(x^i_{OS}) \approx f_{EM}(x^i_{EM}), \qquad \text{for all points } i \qquad (3)$$

where f_{OS} and f_{EM} are the circuit responses simulated by the OS and EM simulators, respectively.

In addition to interconnects, pin assignment optimization at IC packages and connectors have been addressed recently as part of an overall signal integrity task [22]. For connectors the pin assignment problem is two-dimentional (Figure 2),

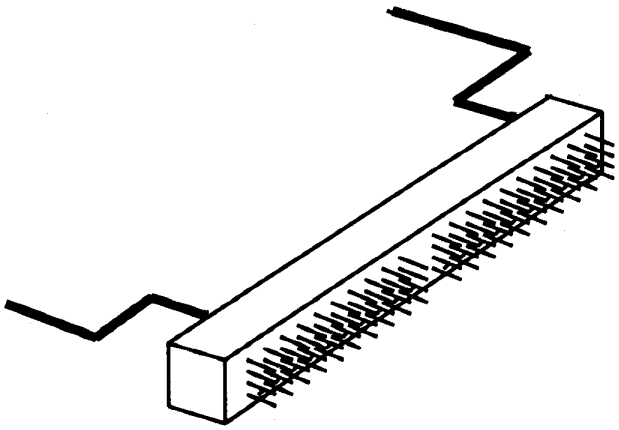

Figure 2. A connector example for 2-dimensional pin-assignment optimization.

and mutual couplings in both dimensions need to be treated. Global optimization techniques including Simulated Anealing and genetic algorithms were used to find optimial pin assignment to minimize crosstalk and ground noise.

With the industrial drive for reduced time to market of new products, the ability of computer-aided design tools to capture various factors during the design stage becomes very important. There has been a significant increase in the complexity of designs, leading to tighter design margins and specifications. Thermal management and signal integrity are the two prominent issues of concern in the design of high-speed systems. One example is multidisciplinary optimization [7] taking into account, e.g., thermal and electrical factors. Let Φ represent the optimization variables. Let $\mathbf{e} = \{e_1, e_2, \ldots, e_m\}$ be a vector containing all the electrical domain error functions as defined in Table I. Let $\mathbf{h} = \{h_1, h_2, \ldots, h_n\}$ be a vector containing all the thermal domain error functions representing the weighted difference between computed and specified temperature at various locations of a circuit board. An objective function $U(\Phi)$ for a generalized two-level l_p and l_q formulation can be defined as

$$U(\Phi) = w_1 [e_1^p + e_2^p + \ldots + e_m^p]^{q/p} + w_2 [h_1^p + h_2^p + \ldots + h_n^p]^{q/p} \quad (4)$$

where w_1 and w_2 are positive weighting factors of the thermal and electrical cost. The optimization is then to find Φ to

$$min\ U(\Phi) \quad (5)$$

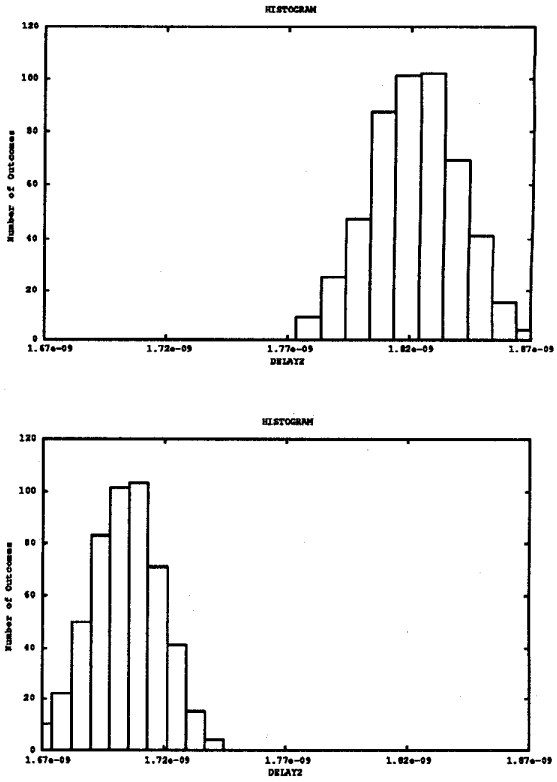

Figure 3. Example of statistical optimization showing histogram of signal delay of an interconnect network before (top figure) and after (bottom figure) yield optimization.

In manufacturability-driven design, it is necessary to consider tolerances in VLSI interconnects and material properties which lead to variations in critical interconnect performances, which in trun can result in reduced production yield. Statistical design [23] techniques address this challenge. Figure 3 is an example of statistical optimization of an interconnect network where the histogram of the delay from an interconnect network are displayed before and after yield optimization. After optimization, the distribution of the delay moved towards the left, leading to generally less delay in the example network.

Conclusions

A review of signal integrity optimization of high-speed VLSI packages and interconnects has been presented. Because of the continuous increase in operating frequency, there is a strong trend in the industry to use signal integrity as one of the fundamental criteria in early design, physical design and postdesign verification. More complete signal integrity design optimization will be a direction of future endeavors.

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