NEXT GENERATION OPTIMIZATION METHODOLOGIES FOR WIRELESS AND MICROWAVE CIRCUIT DESIGN

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ABSTRACT

This paper reviews two exciting concepts: electronic device modeling through artificial neural network technology and circuit optimization exploiting space mapping in the design parameter space. They should play important roles in the next generation engineering optimization methodologies. We elaborate on knowledge based neural network structures for enhanced modeling and aggressive space mapping for efficient electromagnetic optimization.

INTRODUCTION

Commercial CAE systems for high-speed, wireless and microwave circuits and systems are no longer regarded as complete without a variety of design automation capabilities. Computer-integrated manufacturing, including CAD, CAM, information management and decision support systems will be a reality facing the design engineer in the next century.

CAE practices such as active and passive device, circuit and system design are expected to be physically and electromagnetically based, to include electrical, mechanical and thermal effects. Future developments in integrated CAE tools will concurrently link geometry, layout, physical, electromagnetic (EM) and process simulations, with performance, yield, cost, system specifications, manufacturability and testability in a manner transparent to the designer.

In this paper we focus upon two exciting concepts, which we believe will play important roles in the next generation optimization methodologies: device modeling through artificial neural network technology and space mapping optimization.

These technologies are targeted at the design of high-speed VLSI interconnects, large-scale mixed frequency/time domain simulation, chip design, package design, design of multichip modules, printed circuit boards and backplanes, as well as low cost, high-performance RF, microwave and millimeter wave components for system applications.

NEURAL NETWORK MODELING

The need for statistical analysis and yield optimization coupled with the desire to use accurate models such as physics-based and EM-based models leads to tasks that are computationally intensive using conventional approaches. Exploitation of microelectronics CAE models that are both accurate and fast has been a contradictory requirement until neural based models for active and passive elements were introduced [1,2].

Neural networks have the ability to learn from and generalize patterns in data, and to model nonlinear relationships. Neural models can be much faster than original detailed models, more accurate than polynomial and empirical models, allow more dimensions than table lookup models and are easier to develop for a new device/new technology. These appealing features make the neural network a good choice for overcoming some of the difficulties in standard device/circuit modeling and optimization.

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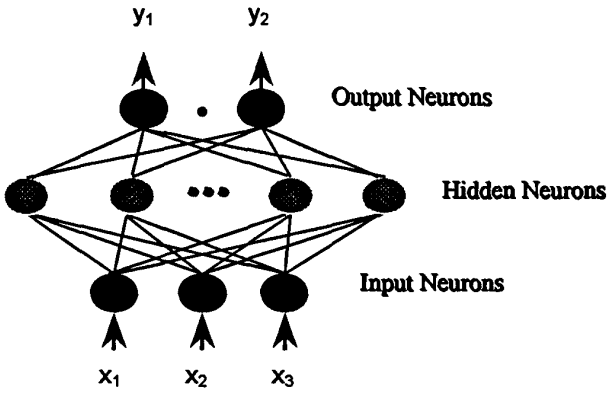

Fig. 1. The multilayer perceptron structure. Shown here is a popularly used three-layer MLP.

Theoretically, a multilayer perceptron (MLP) neural network, as shown in Fig. 1, can model any arbitrary nonlinear relationship between input vector x and output vector y. At the model development stage, sample pairs (x, y), called the training data, are generated from an EM simulation or measurement. The neural model is then trained to learn the input-output (x-y) relationship from the training data. Specifically, training is to determine neural model parameters, i.e., neural network internal weights, such that the neural model predicted output best matches that of the training data. In the model testing stage, a new set of input-output samples, called the testing data, is used to test the accuracy of the neural model.

The ability of neural models to predict accurate y when presented with input parameter values x not seen during training is called the generalization ability. A trained and tested neural model can then be used online during the design stage, providing fast model evaluation replacing original slow EM/device simulators. The benefits of the neural model approach are especially significant when the model is repetitively used such as in circuit optimization, statistical analysis and yield maximization.

Neural networks have been used to develop models for passive components, e.g., transmission lines, and active components, e.g., physics-based MESFETs, in high-speed/high-frequency circuits and systems [2]. EM simulation of coupled transmission lines is slow especially if it needs to be carried out repetitively in the analysis of high speed VLSI interconnects. Neural networks can relate physical parameters, such as conductor width, conductor thickness, directly to electrical parameters, such as cross-sectional RLCG parameters, shown in Fig. 2.

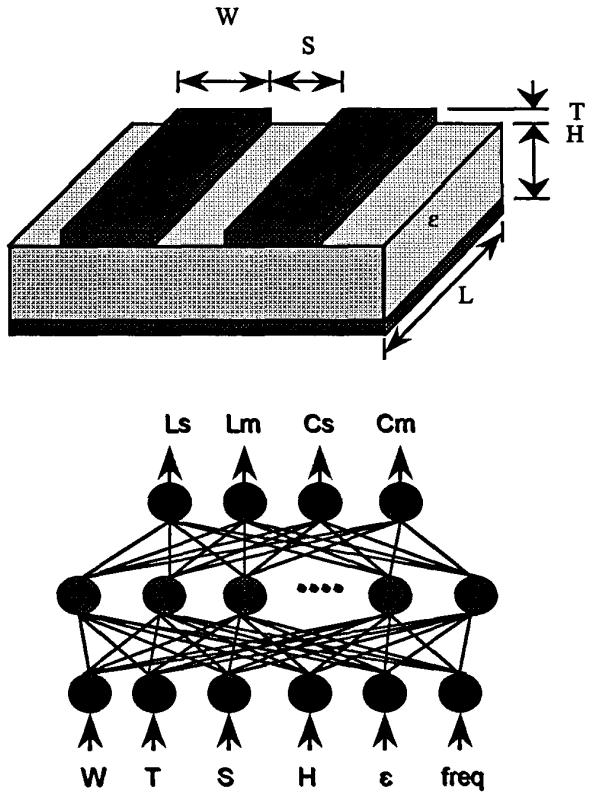

Fig. 2. A neural network model for transmission lines.

Neural models have been found to be several hundreds of times faster than original EM simulations. Physics-based device models of active components require large CPU when used for optimization or iterative simulations. Neural models for MESFETs have been developed with physical parameters as part of the input variables [1,2], as shown in Fig. 3.

In addition to modeling a device or a circuit element, neural networks can also model the entire circuit with the circuit responses as outputs of the models, e.g., a high-speed VLSI interconnect network. A neural model can be developed to predict the signal integrity responses such as signal propagation delays at the terminations [1].

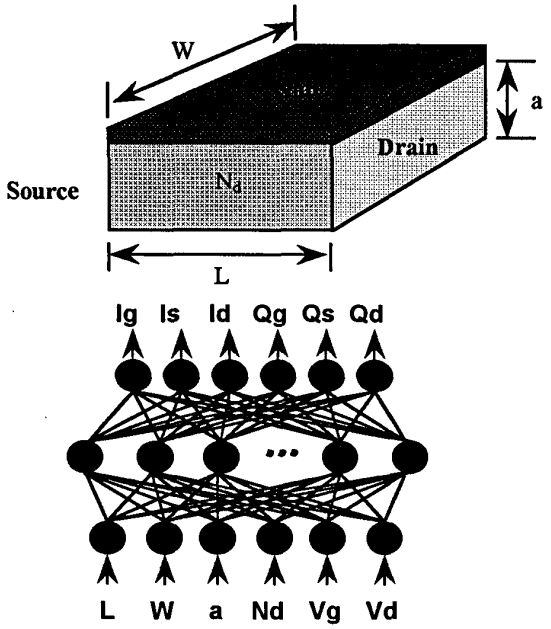

Fig. 3. A neural network model for the physics-based MESFET.

There are emerging demands in the application of neural networks to circuit design, e.g., the reduction in cost of model development and the improvement of model reliability. The developmental cost of neural models comes from the training time of models and training data generation. Fast training algorithms exploiting sparse optimization concepts have been developed to considerably reduce the training time.

A Knowledge Based Neural Network (KBNN) structure has been developed [2] to address these demands more systematically. In this structure, engineering knowledge in the form of empirical functions or analytical approximations is embedded into internal neural network structures. Switching Boundary and Region neurons are introduced in the model structure to reflect engineering concepts where different equations or formulas with different parameters can be interchangeably used in different regions of the input parameter space. This technique enhances neural model accuracy especially for unseen data, reduces the need for large sets of training data, and thus reduces model development cost.

A novel neural based modeling technique for high-speed/high-frequency circuits and systems has been developed. The feasibility and efficiency of neural models have been demonstrated through examples. The proposed KBNN combines engineering empirical knowledge with the learning power of neural networks. With the ultra fast recalling speed of neural models, it will have significant impact on the development of interactive CAD tools.

AGGRESSIVE SPACE MAPPING

Space mapping, similarly to the neural network approach also involves the interplay between two representations of a circuit or device. Here, the aim is to align two different simulation models: the so-called "coarse" model, typically an empirical circuit simulation and a "fine" model, typically a full wave EM simulation. The concept is illustrated in Fig. 4, where the coarse model is called the "optimization" model and the fine model is identified as the "validation" model.

The technique combines the accuracy of the fine (validation) model with the speed of the coarse (optimization) model during the circuit optimization process. Parameter extraction is a crucial part of the technique. During this step the parameters of the coarse model whose response matches the fine model response are obtained. The extracted parameters may not be unique, causing the technique to fail to converge to the optimal design.

An algorithm for aggressive space mapping (ASM) EM optimization [3] has been introduced. Here, we will review the highlights of ASM.

We refer to the vector of parameters of the fine model as x_{em}. The vector of parameters of the coarse model is referred to as x_{os}.

The first step of the ASM technique is to obtain the optimal design of the coarse model x_{os}^*. The technique aims at establishing a mapping P between the two spaces [3]

$$x_{os} = P(x_{em}) \tag{1}$$

such that

$$\|R_{em}(x_{em}) - R_{os}(x_{os})\| \leq \varepsilon \tag{2}$$

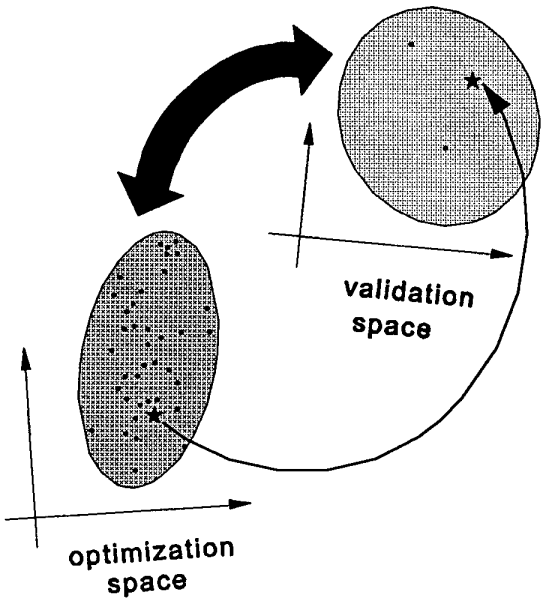

Fig. 4. The concept of aligning two spaces in the space mapping approach.

where R_{em} is the vector of fine model responses, R_{os} is the vector of coarse mode responses and $\| \|$ is a suitable norm. The error function

$$f = P(x_{em}) - x_{os}^{*} \tag{3}$$

is first defined. The final fine model design is obtained and the mapping is established if a solution for the system of nonlinear equations

$$f(x_{em}) = 0 \tag{4}$$

is found.

Let $x_{em}^{(i)}$ be the ith iterate in the solution of (4). The next iterate $x_{em}^{(i+1)}$ is found by a quasi-Newton iteration

$$x_{em}^{(i+1)} = x_{em}^{(i)} + h^{(i)} \tag{5}$$

where $h^{(i)}$ is obtained from

$$B^{(i)} h^{(i)} = -f(x_{em}^{(i)}) \tag{6}$$

and $B^{(i)}$ is an approximation to the Jacobian of the vector f with respect to x_{em} at the ith iteration. The matrix B is updated at each iteration using Broyden's update.

It is seen from (1)-(3) that the vector function f is obtained by evaluating $P(x_{em})$. This can be achieved through the process of parameter extraction. Parameter extraction involves solving a subsidiary optimization problem.

During parameter extraction the parameters of the coarse model whose response matches the fine model response are obtained. It can be formulated as

$$\underset{x_{os}}{minimize} \left\| R_{em}(x_{em}^{(i)}) - R_{os}(x_{os}) \right\|. \tag{7}$$

The extracted parameters may not be unique, causing the space mapping optimization technique to fail.

ASM has been applied to a number of design examples exploiting full wave EM simulators. The Sonnet EM solver *em* has been used to optimize various filters, including the design of a high temperature superconducting filter. The finite element solvers Ansoft and HP HFSS have been used to design various 3D structures such as waveguide transformers and filters. Coarse models for these examples exploited coarse grid EM models or circuit-theoretic/analytical models. Coarse models, decomposed into subnetworks, have even consisted of a mixture of EM based subnetworks and empirical elements connected through circuit theory.

A new ASM algorithm called TRASM (Trust Region Aggressive Space Mapping) automates the selection of fine model points used in a multi-point parameter extraction process [4].

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