

# An Automated Space Mapping Framework

Qingsha S. Cheng, *Member, IEEE*, and John W. Bandler, *Fellow, IEEE*

Simulation Optimization Systems (SOS) Research Laboratory,  
McMaster University, Hamilton, ON, Canada L8S 4K1, www.sos.mcmaster.ca

**Abstract**—In this paper we describe an automated space mapping framework exploiting Agilent ADS. Four key schematics of the framework are introduced. We use the Application Extension Language functions to connect the four schematics. A straightforward methodology is presented for designers to use our approach. We provide examples of a novel “cake-cutting” illustration and a two-section transformer that apply the SM framework.

**Index Terms**—space mapping, electromagnetics-based CAD, circuit design, microwave modeling.

## I. INTRODUCTION

Space Mapping (SM) technology [1] addresses the issue of reducing unnecessary time-consuming full-wave electromagnetic (EM) simulations of microwave structures in device modeling and design optimization. Agilent ADS is a widely-used Electronic Design Automation (EDA) system for high-frequency and microwave modeling and design applications. The first SM implementation in ADS was the implicit SM [2]. Later, we presented a comprehensive microwave design framework [3] for implementing the original, aggressive, implicit, and response-residual space mapping approaches through ADS. We recently presented new advances in microwave and RF device modeling exploiting space mapping technology [4] in Agilent ADS. These techniques are simple but require the user’s constant intervention to transfer data and manually run the next step (schematic) of SM. In this paper we describe a technique to automate the SM process.

## II. AUTOMATED SPACE MAPPING IMPLEMENTATION

Four steps of the space mapping technique are used for input, implicit or output SM implementations.

*Step 1* Coarse model optimization.

*Step 2* Fine model simulation.

*Step 3* Parameter extraction.

*Step 4* Re-optimization of the surrogate.

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Q.S. Cheng is with the Simulation Optimization Systems Research Laboratory, Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada L8S 4K1.

J.W. Bandler is with the Simulation Optimization Systems Research Laboratory, Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada L8S 4K1 and also with Bandler Corporation, Dundas, ON, Canada L9H 5E7.

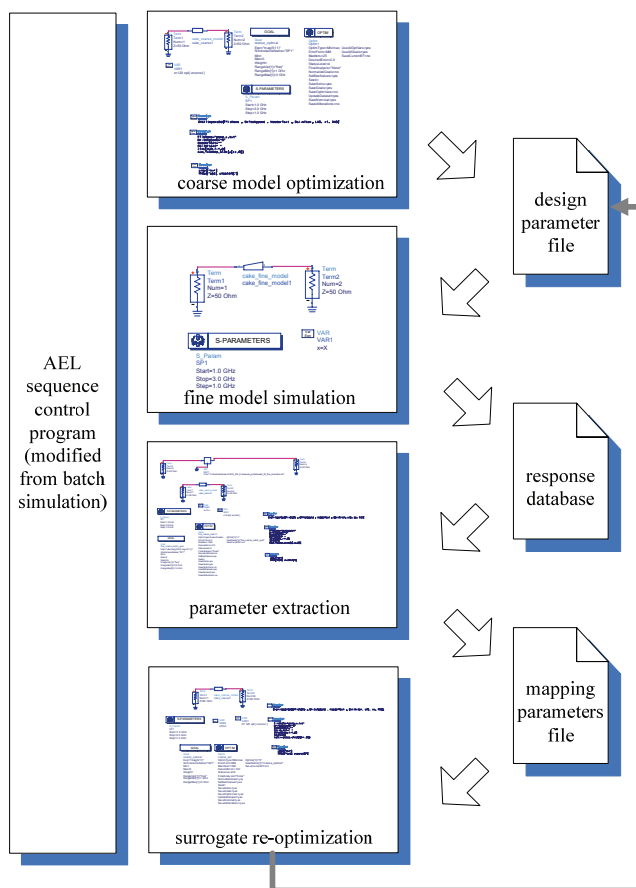


Fig. 1. Automated ADS space mapping framework.

All four steps are connected in our framework as in Fig. 1. Each of the four steps is implemented in an ADS schematic. The coarse model optimization schematic optimizes the coarse model and exports the optimal solution (Fig. 2). *Step 2* simulates the fine model at the optimal solution obtained in the previous step (Fig. 3). In the parameter extraction step, mapping parameters and/or preassigned parameters are extracted to match the surrogate to the fine model response (Fig. 4). The re-optimization schematic loads the mapping parameters or preassigned parameters from the previous step and re-optimizes the surrogate (Fig. 5).

In ADS, the Application Extension Language (AEL) [5] is a general purpose programming language, modeled after the popular C programming language. AEL is used to configure, customize and extend the capabilities of the design environment. Like C, AEL has an extensive set of built-in

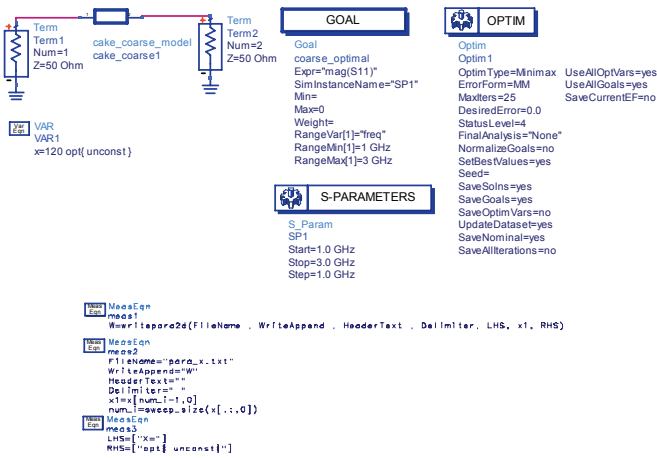


Fig. 2. Coarse model optimization and optimal design parameter export.

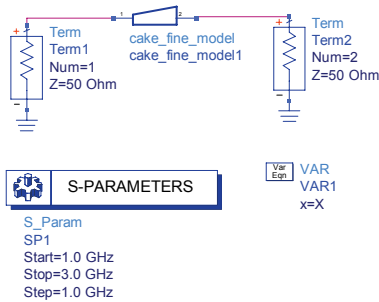


Fig. 3. Fine model simulation.

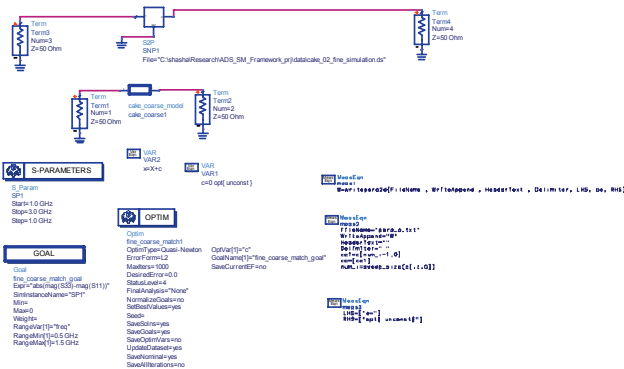


Fig. 4. Parameter extraction.

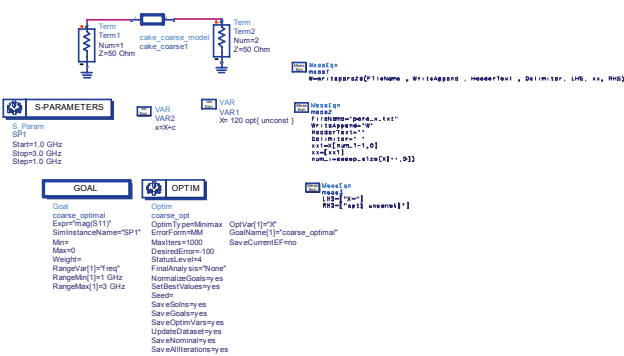


Fig. 5. Re-optimization of the surrogate.

function libraries, including functions for file input/output,

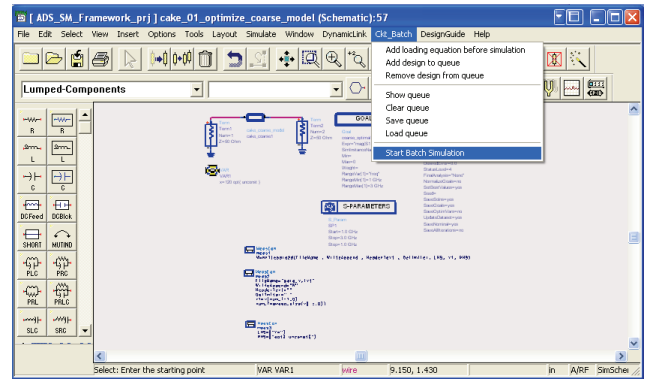


Fig. 6. Menu for the sequence control program (batch simulation).

math, string manipulation, list handling, and database query.

To implement our automated space mapping framework, a few AEL functions are used.

- 1) Sequence control modified from batch simulation.
- 2) Save the optimal values of previous optimization (application of *writepara2d*).
- 3) Load the previous values to the current design schematic (modified from *read\_equations\_from\_file*).

The AEL sequence control is modified from the batch simulation program, Agilent EEsof Knowledge Center Example ID: 8610. This program adds the *Ckt\_batch* menu to the ADS schematic window and provides the capability of sequential simulation of a batch of schematics. To this program we add the equation loading function to fill in the necessary design or mapping parameters before each simulation or optimization starts. We add new menu items and functions to save and load the batch file list (Fig. 6).

To export or save the optimal parameter values we use the *writepara2d* AEL function from Agilent EEsof Knowledge Center Example ID: 142322. The function can save specific information after each schematic simulation (Fig. 7). The saved file has the following format that the next schematic is able to correctly load and use.

X= 129.01 opt{ unconst}

...

To load the equations from a previous schematic, we need to read the file generated by *writepara2d*. An AEL function *read\_equations\_from\_file* from Agilent EEsof Knowledge Center Example ID: 8559 is modified and used. The modification is intended to import multiple equations into one *VAR* component rather than one equation per *VAR*.

The user does not have to understand AEL to use the technique. After loading our modified AEL functions, users

```

MeasEqn meas1
W=writepara2d(FileName , WriteAppend , HeaderText , Delimiter, LHS, x1, RHS)

MeasEqn meas2
FileName="para_x.txt"
WriteAppend="W"
HeaderText=""
Delimiter=" "
x1=x[num,1-1,0]
num_i=sweep_size(x[::,0])

MeasEqn meas3
LHS=["x="]
RHS=["opt{ unconst}"]

```

Fig. 7. Save the design parameters to a file. The file will be loaded by the next schematic.

```

C:/shasha/Research/ADS_SM_Framework_prj } empty line
cake_01_optimize_coarse_model           } coarse model optimization
C:/shasha/Research/ADS_SM_Framework_prj/data/para_x.txt } project folder and name
C:/shasha/Research/ADS_SM_Framework_prj/data/para_x.txt } design parameter file name
C:/shasha/Research/ADS_SM_Framework_prj } fine model simulation
cake_02_fine_simulation                  } project folder and name
C:/shasha/Research/ADS_SM_Framework_prj/data/para_x.txt } design parameter file name
C:/shasha/Research/ADS_SM_Framework_prj } parameter extraction
cake_03_parameter_extraction             } project folder and name
C:/shasha/Research/ADS_SM_Framework_prj/data/para_c.txt } mapping parameter file
C:/shasha/Research/ADS_SM_Framework_prj } re-optimization
cake_04_reoptimization                   } project folder and name
C:/shasha/Research/ADS_SM_Framework_prj/data/para_x.txt } design parameter file name
C:/shasha/Research/ADS_SM_Framework_prj } fine model simulation
cake_02_fine_simulation                  } project folder and name
...

```

Fig. 8. Batch list file for our ADS SM framework.

can implement their own space mapping using the following instructions.

- 1) Create four schematics using the template to adapt the appropriate coarse and fine models, frequency sweep, and variables.
- 2) Edit the list file to specify the folder and design names and parameter file names.
- 3) Click *Load Queue* to load the sequence.
- 4) Click *Start Batch Simulation* to run.

The list file should be in the format shown in Fig. 8. Here we only show the iterations up to two fine model simulations. The user can add more iterations by repeating lines 7 to 15.

### III. EXAMPLES

#### A. “Cake-cutting” Example

Our “fine” model is cylindrical with a slanting top side as in Fig. 9. Our goal is to cut this object into three pieces of equal weight or volume (assume unity density). The first cut is along the line segment  $OA$  where  $O$  is the center of the object

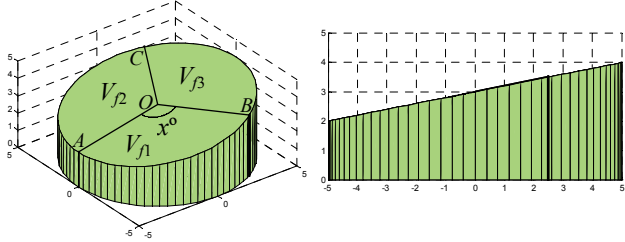


Fig. 9. “Fine” cake model.

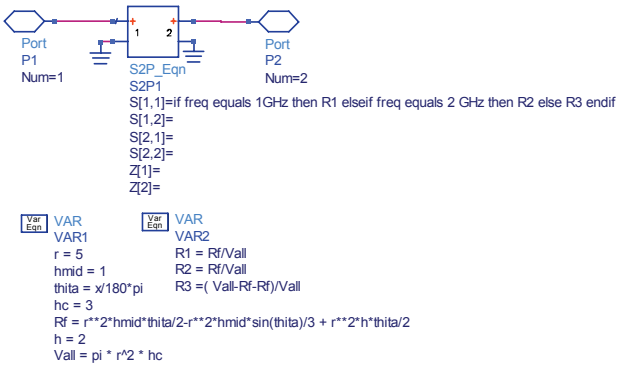


Fig. 10. “Fine” cake model implemented in ADS.

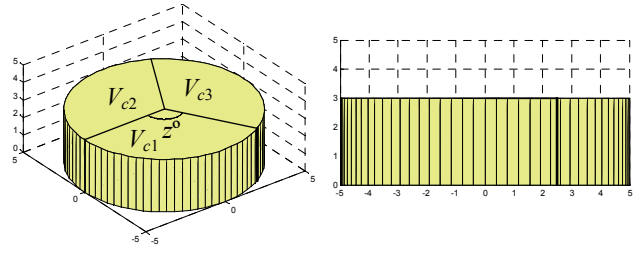


Fig. 11. “Coarse” cake model.

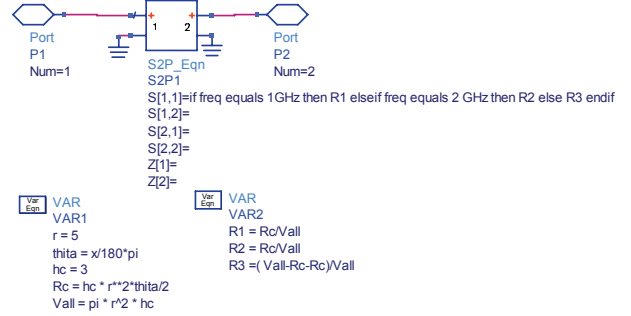


Fig. 12. “Coarse” cake model implemented in ADS.

and  $A$  is the lowest point on the top surface. We decide on  $\angle AOB = x$  where the second cut  $OB$  is applied. The third cut  $OC$  is symmetrical w.r.t. the second cut  $OB$ , i.e.,  $\angle AOB = \angle AOC$ . We implement the model in ADS as shown in Fig. 10.

Our “coarse” model is cylindrical as shown in Fig. 11. The first cut can obviously be anywhere. The second cut has an angle of  $z$  to the first cut. The third cut and the second are symmetrically placed. An ADS representation is shown in Fig. 12.

Optimization of the coarse model gives  $z = 120$ , which yields  $V_c = [V_{c1} V_{c2} V_{c3}] = [0.333 \ 0.333 \ 0.333]V$  where  $V$  is the entire volume of the fine model (the coarse object has the same volume as the fine object). We assign  $x = z$  to the fine model. The fine model yields  $V_f = [V_{f1} V_{f2} V_{f3}] = [0.303 \ 0.303 \ 0.395]V$ . We match the coarse model to the fine model by optimizing the coarse model (surrogate) mapping parameter  $c$ . When  $z + c = 108.97$ , the surrogate matches the fine model volume vector  $V_f$ . Keeping  $c$  fixed we re-optimize the surrogate w.r.t.  $z$ . A new design parameter  $x = 131.03$  is obtained, which gives a fine model “response” of  $V_f = [0.337 \ 0.337 \ 0.325]V$ . We repeat these steps by looping back to the parameter extraction step. In 3 iterations we reach a fine model “response” of  $V_f = [0.333 \ 0.333 \ 0.333]V$ . and  $x = 129.81$ . A step-by-step process is shown in Fig. 13. The “response” after three iterations is shown in Fig. 14.

#### B. Capacitively-loaded 10:1 Impedance Transformer [6]

We consider an ideal two-section transmission line (TL) “coarse” model, and a capacitively-loaded TL “fine” model with capacitors  $C_1=C_2=C_3=10\text{pF}$ . See Fig. 15. The electrical lengths  $L_1$  and  $L_2$  at 1GHz are chosen as design parameters. The frequency range is  $0.5\text{GHz} \leq \omega \leq 1.5\text{GHz}$  with a step of 0.1GHz. The characteristic impedances are kept fixed at the

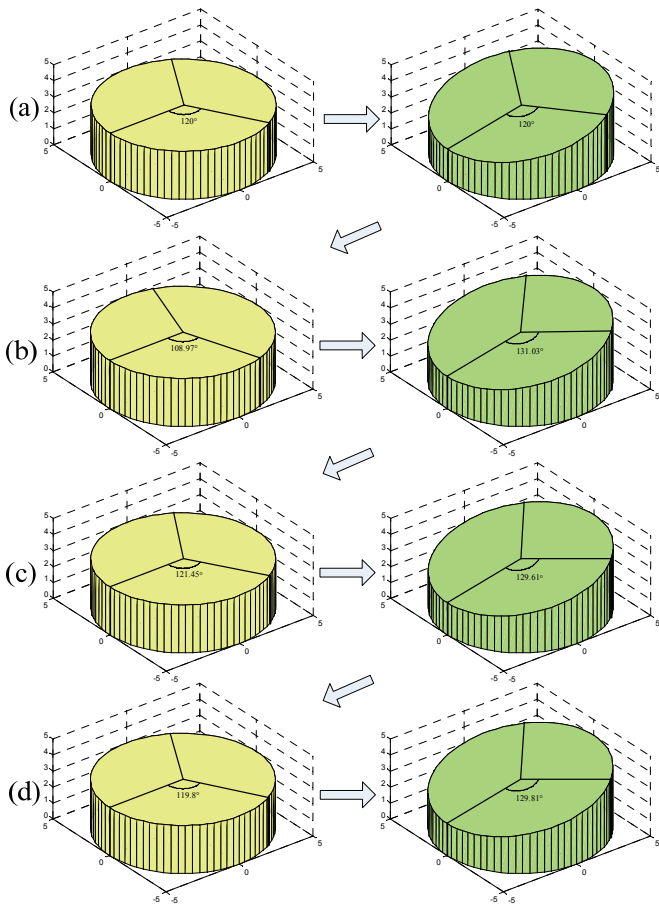


Fig. 13. “Coarse” and “fine” cake models in our ADS SM framework. (a) the initial solution; (b) the first iteration; (c) the second iteration; (d) the third iteration.

optimal values  $Z_1 = 2.2361\Omega$  and  $Z_2 = 4.4721\Omega$ . Both the fine and coarse models are implemented in ADS.

We show that a good response (Fig. 16) is obtained in 4 iterations using our ADS framework. In this example we use input space mapping parameter  $c$  and output space mapping parameter  $d$ .

#### IV. CONCLUSION

We have created a methodology to implement space mapping exploiting Agilent ADS in an automated fashion. Our technique uses 4 ADS schematics corresponding to four SM steps. AEL functions are developed to connect the schematics and to transfer data. A user-defined sequence list file is used to control the space mapping flow. We

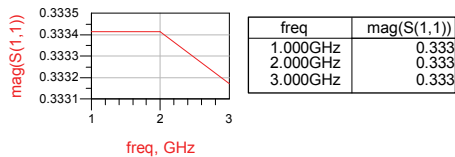


Fig. 14. Fine model “response” in 3 iterations.

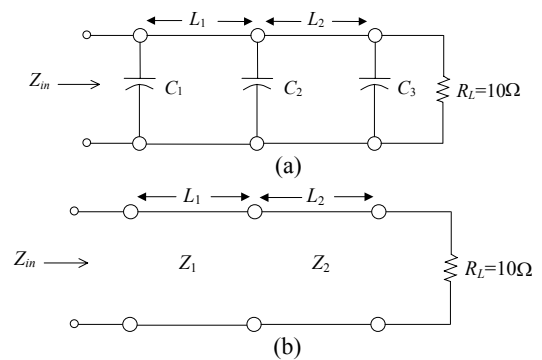
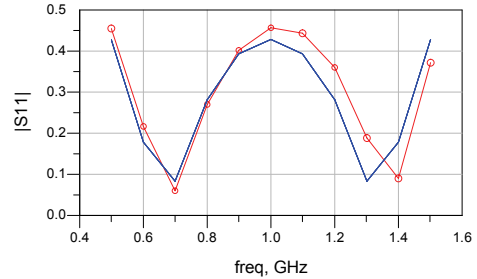


Fig. 15. Two-section capacitively-loaded 10:1 impedance transformer: (a) “fine” model, (b) “coarse” model.



Eqn	$m=\max(\text{mag}(S(1,1)))$	m	Spec_Err
Eqn	$\text{Spec\_Err}=m-0.5$	0.456	-0.044

Fig. 16. The 4th iteration of space mapping, (o) fine model; (—) optimal coarse model.

demonstrate the technique using a novel “cake-cutting” problem and a two-section transformer.

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