# Application Note

## Progress in Simulator-Based Tuning—The Art of Tuning Space Mapping

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Design closure for a filter is the process of going from the initial layout to a layout that when fabricated meets all required specifications. Normally, repeated electromagnetic (EM) analysis is required to achieve design closure. For filters, this process typically requires about two weeks. In contrast, to facilitate rapid design of the filter, port tuning techniques take advantage of auxiliary EM simulations with additional internal ports. With this approach, design closure is achieved with only a few EM analyses and usually requires only one day or so. This technique can be directly applied to planar microwave circuits.

Port tuning is a special case of space mapping. Unlike traditional direct optimization, space mapping technology [1]–[3] takes advantage of a fast surrogate model to drive a CPU-intensive EM model (fine model) to obtain a desirable design in an iterative fashion. The idea is to map designs from fast optimizable circuit models, which we call *surrogate*, to corresponding EM models. Clearly, discrepancies are expected. A parameter extraction step calibrates and updates the surrogate against the EM simulator so that observed differences between the EM and the surrogate simulations are minimized. The surrogate is thereby made ready for subsequent efficient optimization.

In port tuning, additional internal ports are used to insert circuit theory components that are used to tune the circuit. Because the overall circuit response is mostly determined by EM-simulation data, nearly full EM accuracy is realized while, at the same time, the circuit is tuned at very low computational cost. This forms a special case of space mapping that we call tuning space mapping. The port tuning method [4]–[7] employs tunable elements (normally circuit-theory components or interpolated EM component responses) in the EM model (*S*-parameters) to form a surrogate, while surrogates in the conventional space mapping [1]–[3] process are usually pure circuit-theory models or interpolated coarse-grid EM models.

In this article, we discuss the tuning space mapping concept and implementations that encompass the port tuning method. We define multiple auxiliary ports within a structure of interest, e.g., in the manner of the cocalibrated [8] internal ports of an EM simulator [9]. Cocalibrated refers to ports that are perfectly calibrated (i.e., to within numerical precision) and thus insert no error into an EM analysis, critical, for example, for ports placed in the middle of resonators. These ports are calibrated as a group and all ports in a group are referenced to exactly the same, usually global, ground reference. Tuning elements can then be incorporated into the structure using such ports. Tuning space mapping techniques [5], [10], [11] apply tunable (tuning) elements across or between these internal ports [8], [12]. The resulting tunable model constitutes a surrogate for design or modeling purposes.

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## Tuning Space Mapping Procedure

Here, we expand the tuning space mapping procedure beyond that of [11]: as shown in Figure 1, mixed Type 0 and Type 1 embedding can coexist in one surrogate. For Type 0 we insert tuning elements across small or infinitesimal gaps between the added internal ports as in [10]. For Type 1 we replace an entire section of design interest between the internal ports by a tuning element.

In Figure 2(a), we depict a Type 0 tuning space mapping procedure. We start the procedure with an initial design obtained from a circuit model optimization, a filter synthesis tool, or an educated guess. To allow the embedding of tunable elements, we add internal ports to the fine model. We then simulate the fine model with added ports in an EM simulator [9]. We assume the added ports are calibrated so that the error can be neglected [8]. The response is checked against the specification(s). If the specification(s) are satisfied, no further tuning is necessary. If not, we embed appropriate tuning elements into the internal ports of the multiport *S*-parameter file to form a surrogate. We optimize the surrogate to satisfy the specification(s) with respect to the tuning parameters of the embedded tuning elements. We convert the obtained optimal tuning parameters to the corresponding design parameters. After the new design parameter values are calculated or converted, we can simulate the fine model with these new design parameter values and check the responses. The steps can be repeated as needed.

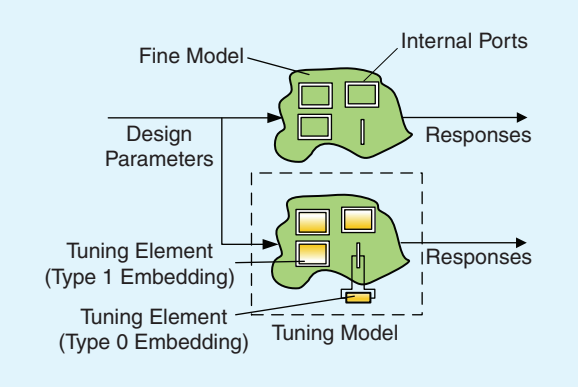


**Figure 1.** *Tuning space mapping and tuning model: mixed Type 1 and Type 0 embedding of tuning elements.*

We show the flowchart of a typical Type 1 tuning space mapping procedure in Figure 2(b). We start the procedure with an initial design similar to Type 0 tuning space mapping. We create and simulate the fine model in an EM simulator. We check if the response of the fine model satisfies the specification(s). If the specification(s) are not met, we create and simulate an auxiliary fine model (the same fine model with added internal ports). We construct a surrogate by embedding tuning elements (using Type 1 embedding) to the auxiliary fine model. We extract certain available parameters (preassigned in the fine model, i.e., preassigned parameters [1], [2]), of the embedded tuning elements or/and mapping parameters of the surrogate to match the response of the fine model. After the extraction, we optimize or tune the surrogate with respect to the tuning parameters to satisfy the specification(s). The tuning parameter values are then converted to a new set of design parameter values if necessary. We can now simulate the fine model with the new design parameter values and check the response. The steps can be repeated as needed.

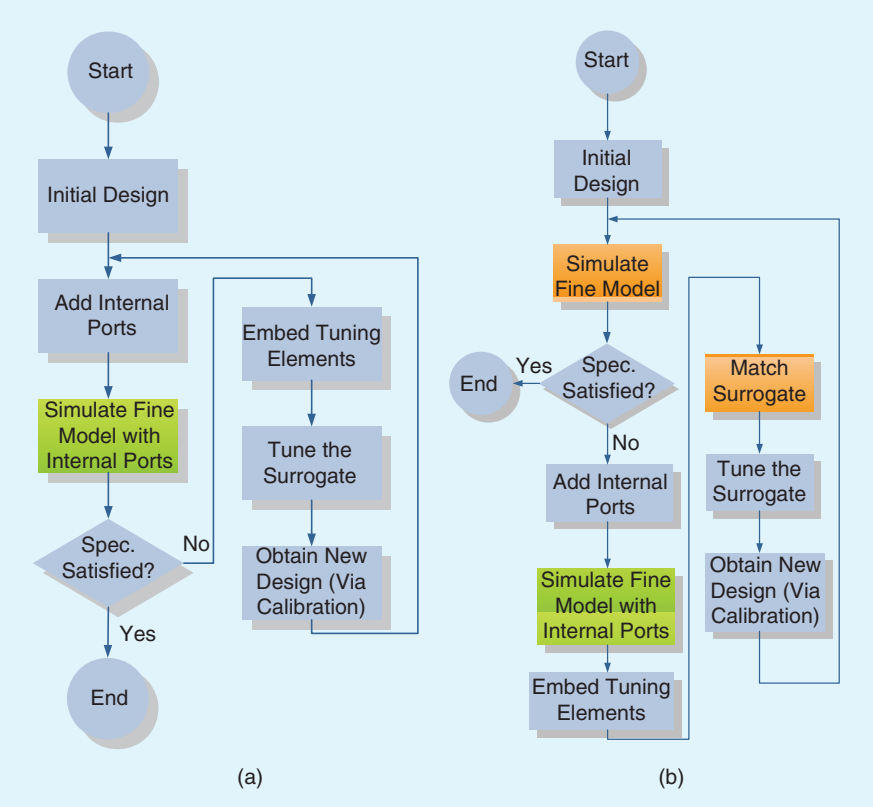


**Figure 2.** *(a) A typical Type 0 tuning space mapping procedure and (b) a typical Type 1 tuning space mapping procedure. The typical Type 1 procedure has two extra steps (shown in orange).*

We can see from Figure 2(a) and (b) that our Type 1 tuning space mapping, with two extra steps colored in orange, is a superset of our typical Type 0 tuning space mapping. The two extra steps are added to compensate for two types of error, port-insertion error

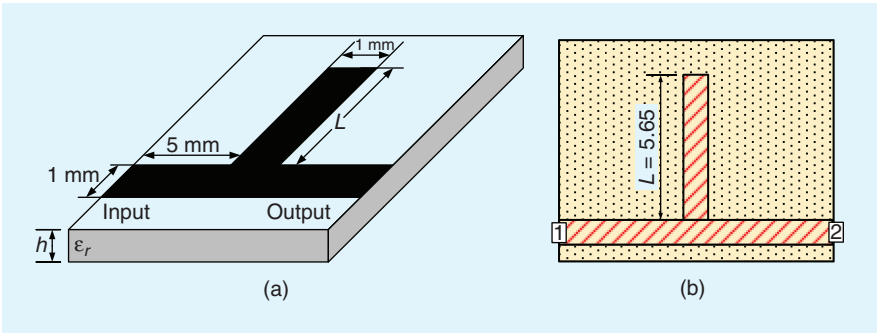


**Figure 3.** *A simple bandstop microstrip filter example: (a) physical structure and (b) the electromagnetic simulator [9] model.*

and tuning-element-insertion error. If the port-insertion error is small enough, e.g., for cocalibrated ports [9], the fine model simulation step may be omitted.

## A Simple Bandstop Filter Illustration

We use a simple bandstop microstrip filter example [1] to illustrate the tuning space mapping. The filter [Figure 3(a)] has only one design parameter, the stub length $L$ (initially 5.65 mm). The goal is to find $L$ so that the center frequency of the filter is 5 GHz. The dielectric constant is ten. The substrate height is 0.5 mm. The fine model is simulated in the EM simulator [9] [Figure 3(b)]. Two types of tuning method are illustrated.

### *Type 0 Tuning*

We slice away a small piece of metal material in the middle of the stub, which leaves a 0.01-mm gap as shown in Figure 4. Two (cocalibrated) internal ports (ports 3 and 4) are created on the edges of the cuts. We simulate this structure as one piece in an EM simulator [9] to obtain its four-port $S$-parameters. We then import the $S$-parameters into a microwave circuit framework [13] and attach an empirical microstrip line model (tuning element) with a length of $t = 0.01$ mm from the circuit library between ports 3 and 4 as shown in Figure 5(a). This is our initial surrogate. We find its responses to be very close to those of the fine model (the original structure without gap or internal ports [Figure 5(b)] as shown in Figure 5(c).

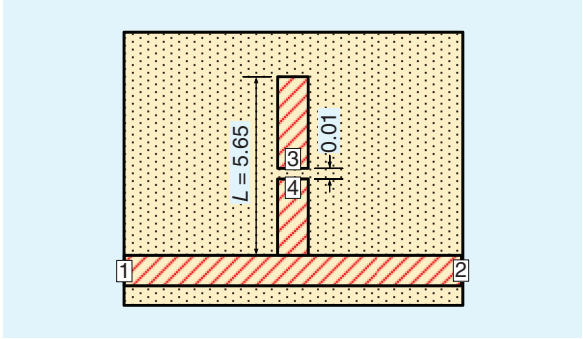


**Figure 4.** *Simple bandstop microstrip filter with internal ports prepared for Type 0 tuning in the electromagnetic simulator [9].*

We tune the length of the attached microstrip line so that the responses of the surrogate satisfy the specification. We obtain a tuning length of $t = -0.124$ mm [Figure 5(d)]. This full length of the stub $L$ is calculated as $5.65\text{ mm} - 0.01\text{ mm} + (-0.124\text{ mm}) = 5.516$ mm. We apply the full length $L$ to the fine model [Figure 5(e)]. After simulation, the responses satisfy the specification [Figure 5(f)].

We tested the Type 0 tuning on the example of Figure 5 using the so-called not de-embedded $S$-parameters (ports are not calibrated). The initial errors are much larger than those shown in Figure 5(c). An extra parameter extraction process is required to match the surrogate to the fine model, yielding an extracted parameter value $t = -0.366$ mm. We then optimized $t$ with respect to the specification, giving $t = -0.510$ mm. Our Type 0 tuning algorithm design now gives $L = 5.65\text{ mm} + (-0.510\text{ mm} - (-0.366\text{ mm})) = 5.506$ mm, a design similar to that of Figure 5(e).

### *Type 1 Tuning*

Now we apply Type 1 tuning. We slice away two pieces of metal material in the stub 0.5 mm away from either end of the stub as shown in Figure 6. We then add (cocalibrated) internal ports to the cut edges. The entire structure is simulated [9] as one piece and a six-port $S$-parameter file is obtained. We import the $S$-parameter file into the circuit simulator [13] and replace the middle piece of the stub with an empirical microstrip line model as shown in Figure 7(a). This is our new surrogate. We extract the dielectric constant of the tuning element in the surrogate to match the responses of the surrogate to the fine model [Figure 7(b)]. We show the responses of surrogate and fine model in Figure 7(c).

Our surrogate with the new dielectric constant is optimized with respect to the tuning parameter $t$. We obtain a tuning parameter of 4.508 mm [Figure 7(d)]. The new design prediction is calculated as $L = 0.5\text{ mm} + 0.5\text{ mm} + 4.508\text{ mm} = 5.508$ mm. We verify this design [9] [Figure 7(e)]. The responses are close to satisfying our specification [Figure 7(f)]. One more iteration is sufficient to bring the EM fine model [9] to a design that satisfies the specification [Figure 7(g)–(i)].

## Examples

### *Narrowband 62 GHz Interdigitated Filter*

We optimize a narrowband 62 GHz interdigitated filter using port tuning (Type 0 embedded tuning space mapping). The design parameters are

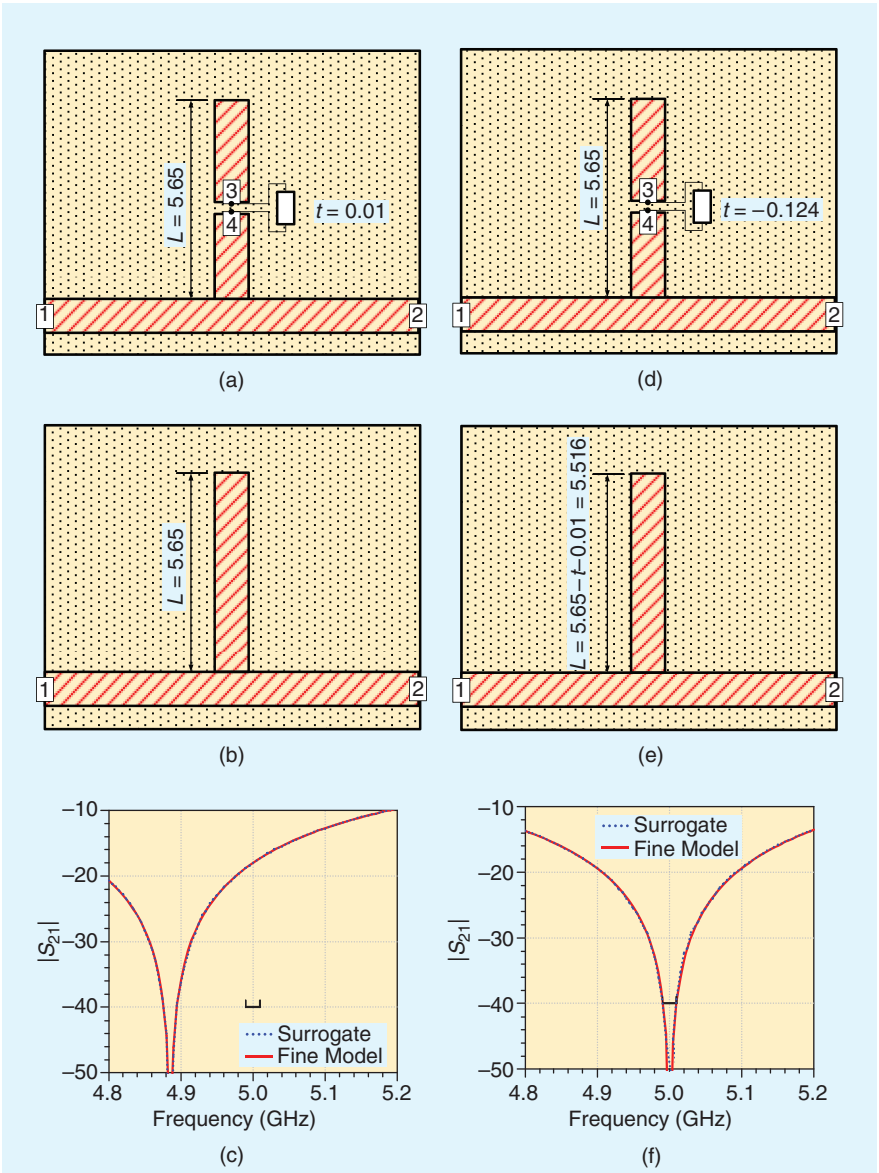


**Figure 5.** *Simple bandstop microstrip filter design using Type 0 tuning space mapping: (a) the surrogate at the initial design, (b) the fine model at the initial design, (c) the responses at the initial design, (d) the surrogate after tuning (optimization), (e) the fine model with a new design parameter value, and (f) the responses of the optimized surrogate and the new fine model design.*

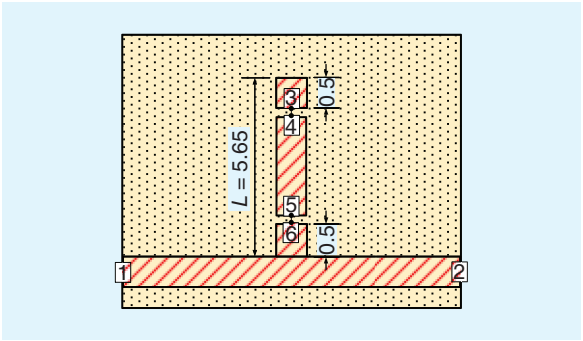


**Figure 6.** *Simple bandstop microstrip filter with internal ports prepared for Type 1 tuning in the EM simulator [9].*

$[\text{Offset } L_1\ L_2\ L_3\ S_1\ S_2]^T$ mm as shown in Figure 8. The specifications are

$$\begin{aligned} |S_{11}| &\le -20 \text{ dB for } 61 \text{ GHz} \\ &\le \text{freq} \le 63 \text{ GHz} \\ |S_{21}| &\le -40 + (\text{freq} - 44) \\ &\quad \cdot 30/15 \text{ dB for } 44 \text{ GHz} \\ &\le \text{freq} \le 59 \text{ GHz} \\ |S_{21}| &\le -10 - (\text{freq} - 65) \\ &\quad \cdot 30/11 \text{ dB for } 65 \text{ GHz} \\ &\le \text{freq} \le 76 \text{ GHz}. \end{aligned}$$

The initial values of the narrowband 62 GHz interdigitated filter design are $[8.5\ 11.5\ 8.5\ 4\ 5\ 4.75]^T$. After the internal ports are inserted, we conduct an EM simulation [9]. In the circuit schematic [14], the tuning model (surrogate) is constructed by importing the EM simulated $S$-parameters and embedding suitable tuning elements. The tuning elements are capacitors (tuning gaps $[S_1\ S_2]^T$) and microstrip lines (tuning lengths and offset $[\text{Offset } L_1\ L_2\ L_3]^T$) as shown in Figure 9. We can now tune the surrogate to satisfy the specifications. The responses of the fine model and the surrogate at the initial design are shown in Figure 10. Here, the fine model is labeled *confirm*. The confirm result is a standard EM simulation of the entire filter prior to inserting any tuning ports. The accuracy of such EM simulations has been verified in prior publications [15], [16]. This is the filter layout that would actually be fabricated once we have it tuned to meet requirements. Agreement between the confirm result and the Tune (or surrogate) result (i.e., the result with tuning ports and circuit theory tuning elements set to yield the original confirm layout dimensions) indicates that we set up the tuning schematic correctly and that the circuit theory elements are working as expected. The small differences are due to the circuit theory transmission lines being near the limits of their validity. Fortunately, circuit theory is only a small part of the Tune result, so the overall errors are small. However, there is still enough accuracy in the circuit theory that they can still be used to tune the filter.

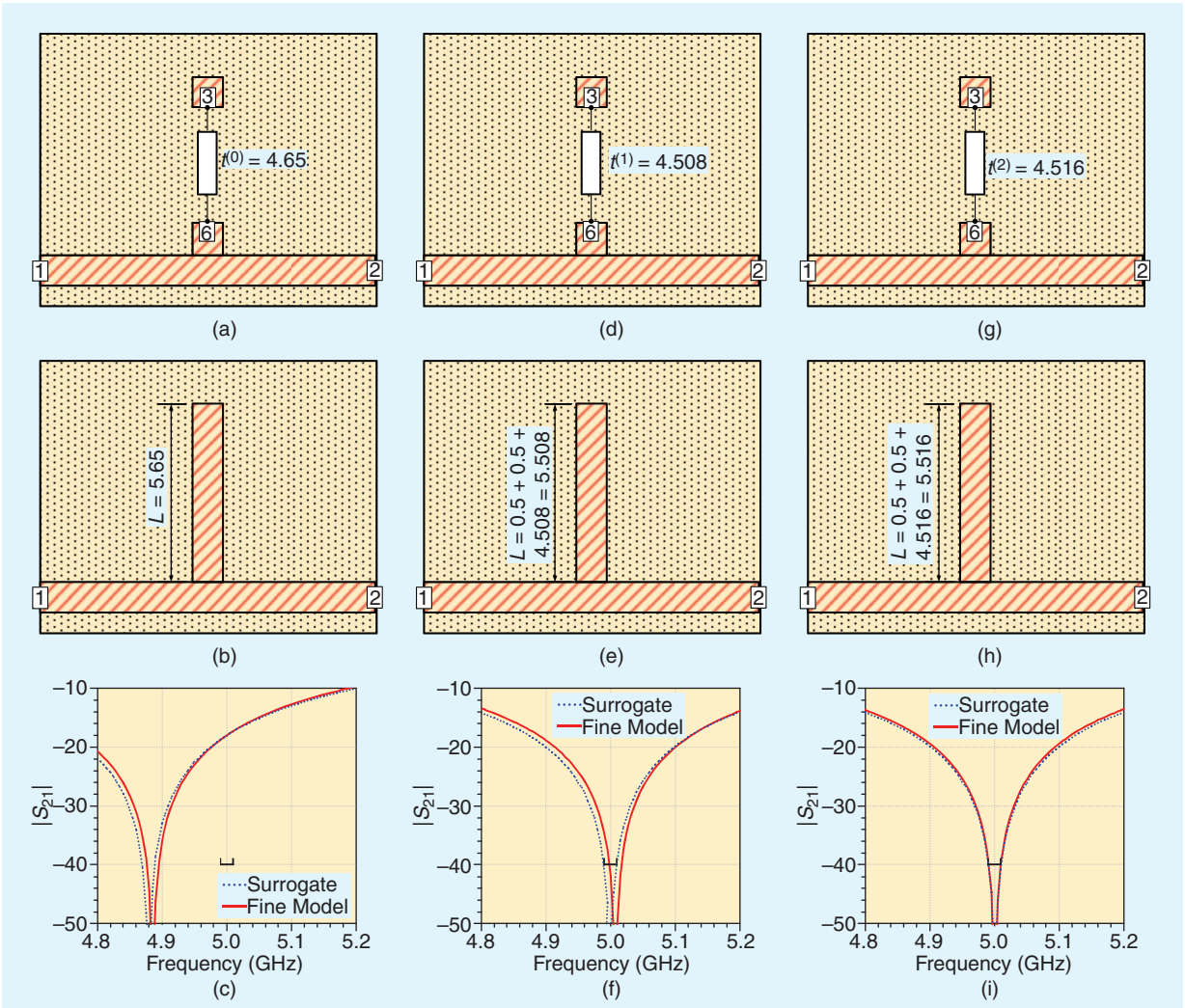


**Figure 7.** *Simple bandstop microstrip filter design using Type 1 tuning space mapping: (a) the surrogate at the initial design, (b) the fine model at the initial design, (c) the responses at the initial design, (d) the surrogate after tuning (optimization), (e) the fine model with a new design parameter value, (f) the responses of the optimized surrogate and new fine model design, and (g)–(i) the surrogate, the fine model and their responses after another iteration of tuning space mapping.*

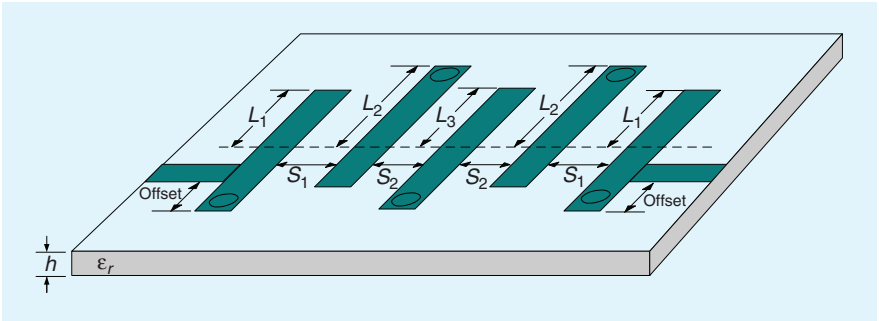


**Figure 8.** *Narrowband 62 GHz interdigitated filter.*

We obtain, in our circuit schematic, a set of optimal parameter values of the tuning elements embedded in the surrogate so that the responses of the surrogate satisfy the specifications. These parameters are capacitances $[C_1\ C_2]^T$ and lengths $[d_0\ d_1\ d_2\ d_3]^T$. We now translate these values to the design parameter values through the following steps. The microstrip lengths $[\text{Offset}\ L_1\ L_2\ L_3]^T$ are obtained by directly adding lengths $[d_0\ d_1\ d_2\ d_3]^T$ to the initial lengths. The capacitance, however, has to be translated into new separations $[S_1, S_2]^T$ using calibration.

We build an interpolated EM submodel using the subsection geometry shown in Figure 11(a). This submodel is simulated sweeping $S_1$ over a large range at 62 GHz. Since the EM submodel is simple, small, and one-dimensional, the interpolation and EM computational costs are moderate. We now construct a subsurrogate using the submodel at the initial value of $S_1$ and the optimal capacitance of $C_1$ as shown in Figure 11(b). A parameter value

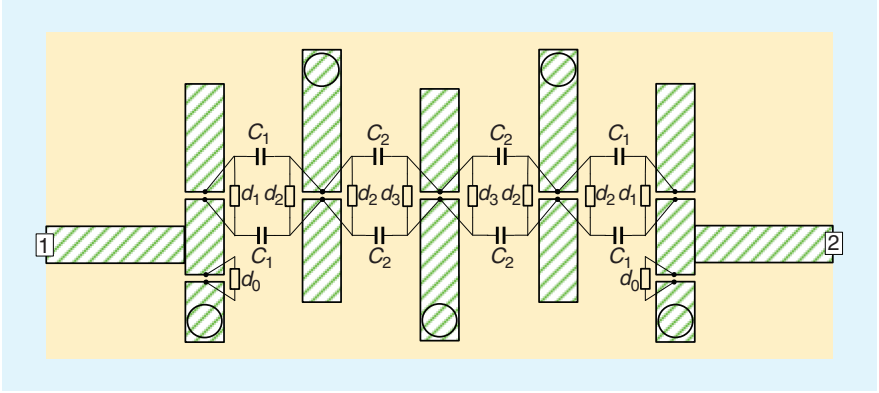


**Figure 9.** *Narrowband 62 GHz interdigitated filter surrogate. The inserted tuning elements are capacitors (as tuning elements for separations) and microstrip lines (for lengths).*

for submodel separation (with interpolation as needed) can be found to match our sub-surrogate [Figure 11(c)]. This is our new separation design for $S_1$. Separations corresponding to the optimal capacitance of $C_2$ can be found the same way. We now have new values for all design parameters and we confirm the new design; see Figure 12. After repeating the entire process (including the calibration step) one more time, the specifications are satisfied as shown in Figure 13.

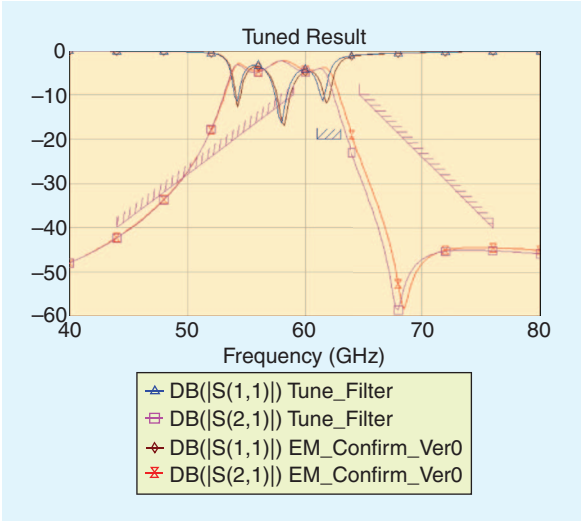


**Figure 10.** *The narrowband 62 GHz interdigitated filter initial responses.*

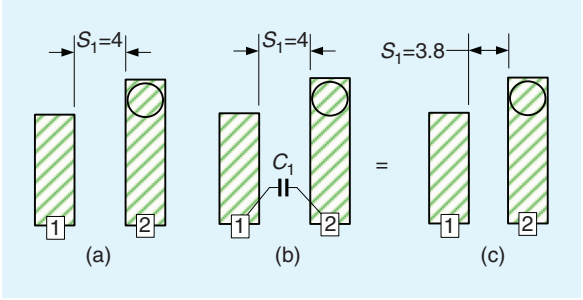


**Figure 11.** *The calibration process converts the capacitance to the separation between the lines using an interpolated partial fine model: (a) a submodel at the initial design, (b) a subsurrogate with attached capacitor at the optimal capacitance value, and (c) the corresponding interpolated EM submodel.*

## Open-Loop Ring Resonator Bandpass Filter

In [11], an open-loop ring resonator bandpass filter [17] was designed using Type 1 elements. Here, we apply our expanded, mixed Type 0/Type 1 approach.

As shown in Figure 14, our design parameters are $x = [L_1\ L_2\ L_3\ L_4\ S_1\ S_2\ g]^T$ mm. See [11] for other parameters and design specifications.

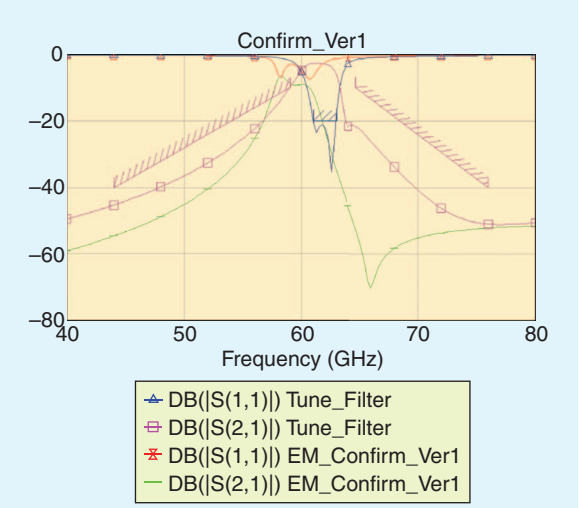


**Figure 12.** *The narrowband 62 GHz interdigitated filter after one iteration.*

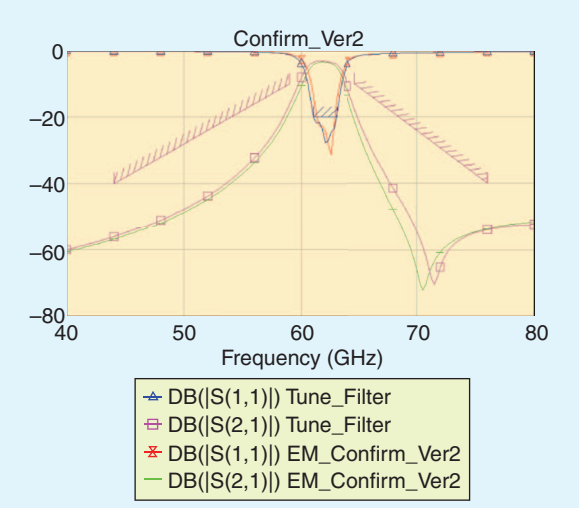


**Figure 13.** *The narrowband 62 GHz interdigitated filter after two iterations. The specifications are satisfied.*

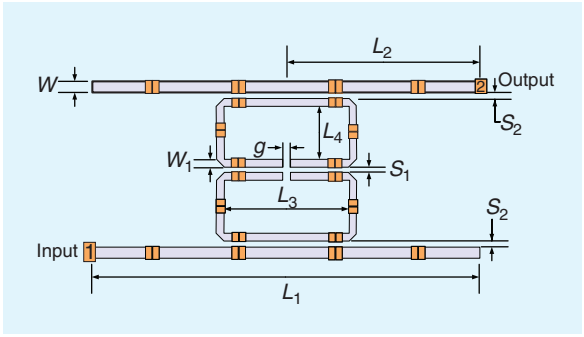


**Figure 14.** *The open-loop ring resonator bandpass filter: physical structure with cocalibrated ports inserted.*

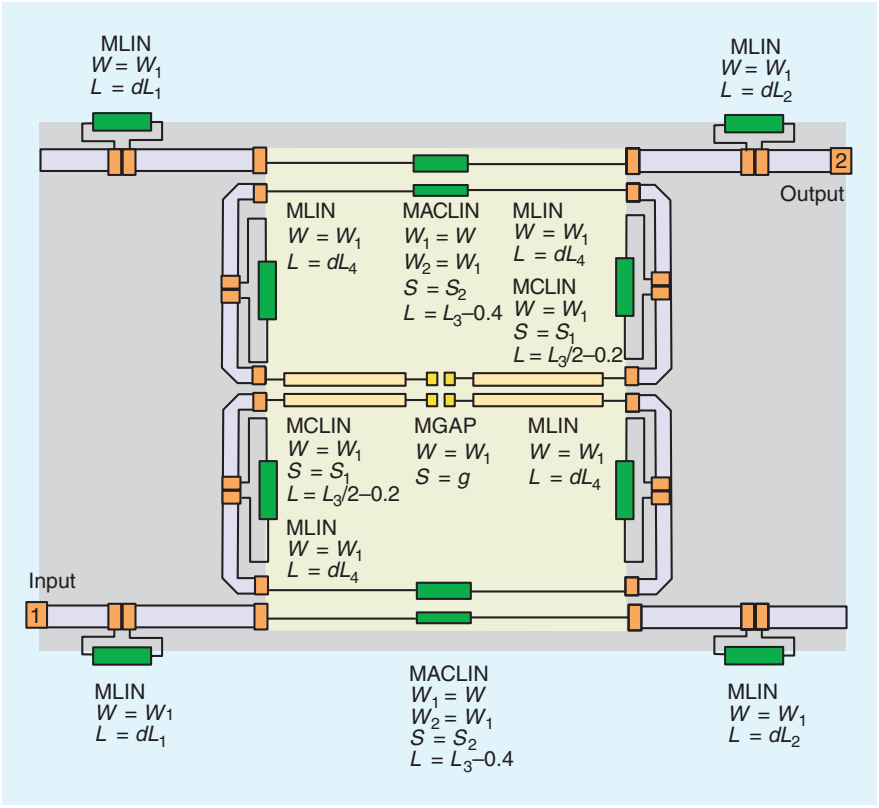


**Figure 15.** *The open-loop ring resonator bandpass filter realized in the circuit simulator [13] using mixed Type 0 and Type 1 embedding.*

The fine model is simulated in the EM simulator [9], while the tuning model is constructed and optimized in the microwave circuit framework [13]. We divide the microstrip structure and insert cocalibrated port pairs at the cut edges as shown in Figure 14. Then we simulate the auxiliary EM structure with the ports and import the resulting SNP data file (50 ports) as an SNP *S*-parameter component into the circuit simulator [13]. Equivalent circuit microstrip lines (Type 0) are inserted and microstrip coupled-line and gap components (Type 1) replace sections of the structure in Figure 15. A new tuning model is now available with parameters $[dL_1\ dL_2\ dL_3\ dL_4\ S_1\ S_2\ g]^T$ mm.

The initial guess is $x^{(0)} = [25.4\ 12.6\ 4.8\ 3.6\ 0.2\ 0.1\ 0.6]^T$ mm. Figure 16 shows the responses of our tuning model, our fine model, and the fine model with cocalibrated ports. As in [11], deviations between the tuning model and fine model are compensated by calibrating the dielectric constant and substrate height or length offsets of the tuning elements.

After compensation, the tuning model or surrogate is seen as a better representation of the fine model and is optimized by a circuit simulator [13] with respect to the design parameters. The new design parameters are then assigned to the fine model. The optimal values obtained are $x^{(2)} = [20.34\ 7.72\ 6.94\ 2.97\ 0.34\ 0.26\ 0.85]^T$ mm, after two iterations. The optimized tuning model and the corresponding fine model responses are shown in Figure 17.

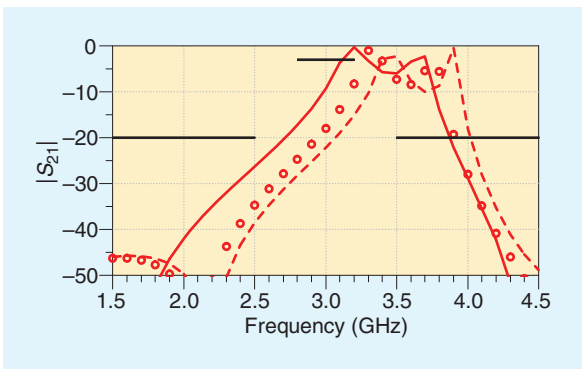


**Figure 16.** *Initial responses: tuning model (red solid line), fine model (red circles), and the fine model with cocalibrated ports (red dashed line).*

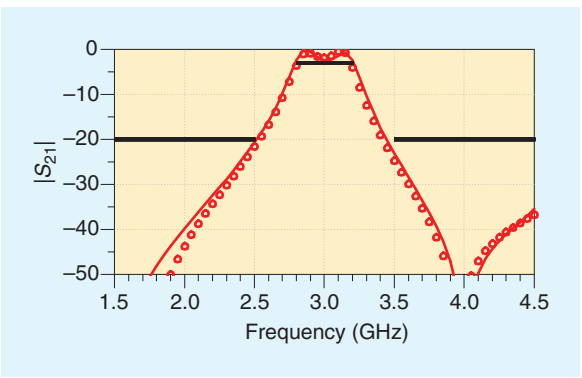


**Figure 17.** *Responses after two iterations: the tuning model (red solid line) and the corresponding fine model (red circles).*

## Discussion

In this section, we discuss the port-tuning technique from a physics point of view. We flag certain aspects that might need attention when applying the technique. We also discuss issues of interest to microwave engineers, some of which remain open for further exploration.

### *Location of the Cuts*

The cuts for port tuning should be typically made at least one substrate thickness or line width (whichever is greater) away from any other discontinuities in the circuit being tuned. This is because the cocalibrated port calibration does not remove interaction between the ports and any very nearby discontinuities. If our situation requires the very highest accuracy, then such fringing field coupling could cause problems. We should also take special care to minimize the number of variables. While this is well known among experienced designers, new designers sometimes find themselves learning this the hard way. For example, if a filter is symmetric (i.e., looks the same when we swap the input and output ports), we can significantly reduce the number of optimization variables by reusing the input side optimization variables on the output side.

### *Effect of Cutting and Reconnection*

Making the cuts and then reconnecting the removed circuitry have negligible effect on the circuit response provided 1) the port connecting lines are not over-moded, 2) the coupling between the removed portion and the rest of the circuit is not significant, and 3) the *S*-parameters that replace the removed portion of the circuit are accurate.

As for the first condition, we need to make sure that the port connecting lines are not, for example, one half wavelength wide. In this case, higher-order modes can propagate and the calibration fails. Also, as mentioned above, we must make sure the ports are far enough from other circuit discontinuities so that their fringing fields do not interact. This is also higher-order-mode coupling. As for the second condition, if we remove a large length of coupled line, for example, and replace it with two uncoupled transmission lines, there would be a large error. However, if the length of line removed and then replaced is very short (i.e., we are tuning the length over a small range), then the introduced error is small and may perhaps be acceptable. For the third condition, we have found, especially at high frequency, that (uncalibrated) circuit theory models in popular microwave EDA tools start to fail (often indicated by warning messages displayed by the tool). If we use such (uncalibrated) circuit theory models, then the port tuning methodology also fails. In this case, we must use either calibrated elements or substitute pure EM for the tuning elements.

### *Model with Internal Cuts Versus Combination of Submodels*

A model with cuts for tuning ports includes all coupling between all parts of the circuit except those parts that have been removed and replaced by tuning ports. A model that is simply composed of numerous submodels includes no coupling between the submodels. The designer must consider this when deciding how to proceed.

## Conclusions

We discuss tuning space mapping (port-tuning) techniques that can significantly reduce time and effort for design closure. We elaborate on various possible approaches. We distinguish between Type 1 and Type 0 embedding to indicate how tuning elements may be introduced into EM simulations to form suitable tuning models or surrogates. We optimize and update such surrogates iteratively to predict good EM designs. We illustrate the techniques using a simple bandstop filter and demonstrate their power using more complex filter design examples. Finally, we discuss from a physics point of view the possible locations of cuts, the effects of the cutting and reconnection, and we compare models that employ internal cuts with models that consider combinations of submodels.

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