INTEGRATED APPROACH TO MICROWAVE DESIGN

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Abstract

A new concept of practical design applicable to microwave circuits and involving, in general, simultaneous centering, tolerancing and tuning is presented. The worst-case tolerance problem falls out as a special case. With such an integrated approach, designs previously regarded as unrealistic might be made more attractive. Practical implementation involving, for example, nonideal components and uncertain reference planes is also treated in this paper from the tolerance point of view.

Introduction

Component tolerance assignment is now considered to be an integral part of the design process[1-7]. The optimal worst-case tolerance problem with variable nominal point has benefitted significantly in terms of increased tolerances obtained[3-6]. Tuning is known to be very important in microwave design. This work, therefore, brings in the tuning of one or more circuit components basically to further increase tolerances to reduce cost or to make unrealistically toleranced solutions more attractive. This new approach embodies centering, tolerancing and tuning in a unified formulation at the design stage[8]. The worst-case purely toleranced problem and purely tuned problem fall out as special cases.

The general problem is both mathematically and computationally complicated, much more so than the conventional computer-aided design approach which seeks a single nominal design best satisfying performance specifications subject to other design constraints. The latter approach, however, would normally be used to find a starting point for the work we have in mind.

The Tolerance-Tuning Problem

The problem we are considering may, in general, be stated as: minimize a cost function $C(\underset{\sim}{\phi}^o, \underset{\sim}{\varepsilon}, \underset{\sim}{t})$, subject to $\underset{\sim}{\phi} \in R_c$, where $\underset{\sim}{\phi}^o \triangleq [\phi_1^o\ \phi_2^o \ldots \phi_k^o]^T \geq \underset{\sim}{0}$, $\underset{\sim}{\varepsilon} \triangleq [\varepsilon_1\ \varepsilon_2 \ldots \varepsilon_k]^T \geq \underset{\sim}{0}$ and $\underset{\sim}{t} \triangleq [t_1\ t_2 \ldots t_k]^T \geq \underset{\sim}{0}$. k is the number of designable parameters, $\underset{\sim}{\phi}^o$ is the nominal point, $\underset{\sim}{\varepsilon}$ is the tolerance vector and $\underset{\sim}{t}$ is the tuning vector. Let $\underset{\sim}{E}$ and $\underset{\sim}{T}$ be the k x k diagonal matrices with diagonal elements set to ε_i and t_i, respectively. Then

$$\underset{\sim}{\phi} = \underset{\sim}{\phi}^o + \underset{\sim}{E}\underset{\sim}{\mu} + \underset{\sim}{T}\underset{\sim}{\rho} \quad \in R_c$$

for all $-1 \leq \mu_i \leq 1$ and some $-1 \leq \rho_i \leq 1$. R_c is the constraint region defined by m nonlinear inequality constraint functions of $\underset{\sim}{\phi}$ given by $R_c \triangleq \{\underset{\sim}{\phi} | g_i(\underset{\sim}{\phi}) \geq 0, i = 1,2,\ldots,m\}$. The cost function is chosen, in general, to maximize the tolerances and minimize the tuning range.

To reduce the computational complexity of the problem, and also from a practical point of view, we separate the components into effectively tuned and effectively toleranced parameters. Thus

$$\phi_i = \phi_i^o + \begin{cases} \varepsilon_i' \mu_i & \text{for } \varepsilon_i' \triangleq \varepsilon_i - t_i > 0 \\ t_i' \rho_i & \text{for } t_i' \triangleq t_i - \varepsilon_i \geq 0 \end{cases}$$

under the same restrictions that $-1 \leq \mu_i \leq 1$ and $-1 \leq \rho_i' \leq 1$.

A geometric interpretation of the simplified problem employs the concept of projection. Tuning within a tuning range may be mathematically regarded as the projection of points within the tuning range on the subspace spanned by the toleranced parameters. The result of this will be, then, equivalent to solving a purely toleranced problem in the projected subspace. Furthermore, if the projected region satisfies certain convexity assumptions, only the vertices of the projected region need be considered[6]. Thus, instead of considering $g_i(\underset{\sim}{\phi}) \geq 0$, i = 1,2,...,m, for every possible outcome, we might then take the constraints of the form[8]

$$g_i(\underset{\sim}{P}\underset{\sim}{\phi}^\ell + \sum_{j \in I_t} (\phi_j^o + t_j'\rho_j')\,\underset{\sim}{e}_j) \geq 0, \quad i = 1,2,\ldots,m$$

where $\underset{\sim}{\phi}^\ell$ denotes a chosen vertex[6], $\underset{\sim}{e}_j$ is the jth unit vector, I_t is the index set for the effective tuning components and $\underset{\sim}{P}$ is a k x k diagonal matrix with $p_{ii}=1$ except for $i \in I_t$, in which case $p_{ii}=0$.

If I_t is empty, $\underset{\sim}{P}$ is a unit matrix and the problem is the purely toleranced problem.

Examples

A two-section lossless transmission-line transformer with quarter-wave length sections and source to load impedance of 10 : 1 and 100% relative bandwidth is used as an illustration of the concepts[6]. See Table I for the specifications. Some results are shown in Table II. As expected, tuning of any element enhances all the tolerances. Furthermore, if tuning is expensive it will be rejected by the formulation. The original formulation, though more complicated computationally, is useful if the designer has no idea which components are to be toleranced or tuned.

As a more realistic example we consider a one-section transformer on stripline from 50 to 20Ω. The physical circuit and its equivalent network are shown in Fig. 1. The specifications are listed in Table III. The physical dimensions w_1, w_2, w_3, and ℓ are the design variables. The cost function shown in Table IV is minimized taking into account

(1) parasitic inductances due to step discontinuities
(2) tolerances on $w_1, w_2, w_3, \ell, \varepsilon_r$ (the dielectric

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constant), t_s (the strip thickness), and b (the substrate thickness)

(3) uncertainties in modelling of the parasitics and electrical line parameters

(4) mismatched source and load, represented by reflection coefficients of known maximum magnitude and arbitrary phase (e.g., imperfect connectors).

Tolerances on ε_r, t_s and b are independently imposed on each of the 3 stripline sections. The range of possible values for each of these three quantities is the same for all sections, but the actual outcomes within these ranges could be different.

Explicit formulas for the worst-case reflection coefficient for all possible source and load mismatches were used. The worst possible phase was chosen independently with respect to frequency to accommodate completely general connectors and other adjacent element imperfections. At each frequency, the worst interpretation of source and load mismatch was assumed, taking into account the actual characteristic impedance values being considered of the input and output lines.

Formulas for the parasitics were taken from Nalbandian and Steenaart[9]. The parasitic equivalent circuit was calculated on the basis of the average values of $\sqrt{\varepsilon_r}$, t_s and b across a particular junction. The model uncertainties were conservatively estimated from published experimental results[9,10].

A worst-case study has been made to select a reasonable number of constraints. We generalize the problem to allow for

(1) tolerances on the 13 physical parameters (w_1, w_2, w_3, ℓ, and ε_r, t_s and b for each of the 3 sections)

(2) uncertainties on the 6 model parameters D_1, D_2, D_3, L_1, L_2 and ℓ_t treated as tolerances, where D_i is the effective line width of the ith section.

These 2^{19} sets of extreme values could be considered candidates for the worst case. The vertex selection procedure for the 13 physical parameters follows Bandler et. al.[6] From each of the selected vertices the worst values of the modelling parameters are chosen. After each optimization this selection procedure is repeated, new constraints being added, if necessary.

Results on centering and tolerancing using DISOPT[11] are shown in Table IV. We note that the final number of constraints used is 18. Seven runs were needed to identify the final constraints. About two minutes on the CDC 6400 are required altogether. To verify that the solution meets the specification, the constraint selection procedure was repeated at 21 points in the band.

TABLE I

TWO-SECTION 10:1 QUARTER-WAVE TRANSFORMER

Relative Bandwidth	Sample Points (GHz)	Reflection Coefficient Specification	Type
100%	0.5,0.6,...,1.5	0.55	upper
	Minimax solution (no tolerances)	$\|\rho\|$=0.4286	

Conclusions

The concepts we have derived and the results obtained are promising. It is felt that our approach represents not only an advance in computer-aided design but is currently the most direct way of obtaining minimum cost designs under practical situations, at least in the worst-case sense.

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TABLE III

ONE-SECTION STRIPLINE TRANSFORMER

Center Frequency	5 GHz
Frequency Band	4.5-5.5 GHz
Reflection Coefficient Specification	0.25 (upper)
Source Impedance	50 Ω (nominal)
Load Impedance	20 Ω (nominal)
Source Mismatch	0.025 (ref. coe.)
Load Mismatch	0.025 (ref. coe.)
ε_r	2.54 ± 1%
b	6.35 mm ± 1%
t_s	0.051 mm ± 5%
Uncertainty on L_1, L_2	3%
D_1, D_2, D_3	1%
ℓ_t	1 mm

TABLE II
TWO-SECTION 10:1 QUARTER-WAVE TRANSFORMER
DESIGN CENTERING, TOLERANCING AND TUNING

Cost Function* Parameters	C_1	C_1	C_1	C_2	C_3	C_4	C_5
Z_1^o	2.1487	2.0340	2.2754	2.5025	1.8748	2.1487	2.1487
Z_2^o	4.7307	4.5355	4.9467	5.3337	4.2642	4.7307	4.7307
ε_1/Z_1^o x 100%	12.74	17.83	17.60	25.08	31.62	31.62	12.74
ε_2/Z_2^o x 100%	12.74	17.60	17.83	31.62	25.08	31.62	12.74
t_1/Z_1^o x 100%	-	10.00	-	-	31.62	18.88	0.00
t_2/Z_2^o x 100%	-	-	10.00	31.62	-	18.88	0.00
ε_1'/Z_1^o x 100%	-	7.83	-	-	0.00	12.74	12.74
ε_2'/Z_2^o x 100%	-	-	7.83	0.00	-	12.74	12.74

*$C_1=Z_1^o/\varepsilon_1+Z_2^o/\varepsilon_2$, $C_2=Z_1^o/\varepsilon_1+Z_2^o/\varepsilon_2+10(t_2/Z_2^o)$, $C_3=Z_1^o/\varepsilon_1+Z_2^o/\varepsilon_2+10(t_1/Z_1^o)$, $C_4=Z_1^o/\varepsilon_1+Z_2^o/\varepsilon_2+10(t_1/Z_1^o+t_2/Z_2^o)$
$C_5=Z_1^o/\varepsilon_1+Z_2^o/\varepsilon_2+500(t_1/Z_1^o+t_2/Z_2^o)$

TABLE IV
RESULTS FOR ONE-SECTION STRIPLINE TRANSFORMER

Cost Function	$\frac{1}{100}\left(\frac{w_1^o}{\varepsilon_{w_1}}+\frac{w_2^o}{\varepsilon_{w_2}}+\frac{w_3^o}{\varepsilon_{w_3}}+\frac{\ell^o}{\varepsilon_\ell}\right)$
Sample Points	4.5, 5.5 GHz
No. of Variables	8
No. of Final Constraints	18
Minimal Cost	4.82
w_1^o	4.660 mm
w_2^o	8.968 mm
w_3^o	15.463 mm
ℓ^o	8.457 mm
ε_{w_1}/w_1^o x 100	0.94 %
ε_{w_2}/w_2^o x 100	1.20 %
ε_{w_3}/w_3^o x 100	0.74 %
ε_ℓ/ℓ^o x 100	0.64 %

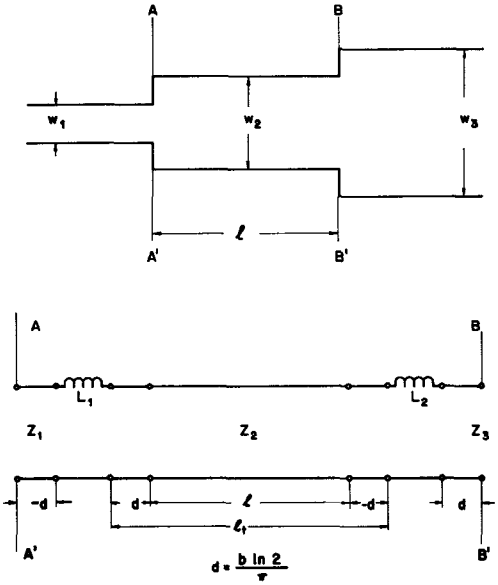

Fig. 1. Stripline transformer and equivalent circuit.